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APPENDIX F

PM RECEIVER

Submitted as part of the Final Report

for RF Test Console on JPL

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NAS 7-100

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WESTINGHOUSE DEFENSE AND SPACE CENTER

SURFACE DIVISION

ADVANCED DEVELOPMENT ENGINEERING

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PM RECEIVER REPORT

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Outline P.M. Receiver Study

1.0 Statement of Work

(3) Perform an analysis of a PM receiver which satisfies the requirements of JPL Specification GPC-15062-DSN, paragraph 3.5.1. The analysis shall include the tracking loop design and an investigation of the achievable dynamic range of the demodulator wideband phase detector. The analysis shall yield a block diagram indicating [illegible] levels and the dynamic range of signal and noise voltages.

(4) Concentrate the P.M. receiver experimentation on the wideband detector, the tracking loop and [illegible] to the extent sufficient to support a valid PM receiver design plan during a later implementation phase.

2.0 Introduction

The P.M. Receiver block diagram is included in Section 2.1. Section 2.3 and 2.4 deal with the detailed signal and noise power levels throughout the receiver and their relationship to the S/N matrices.

Further, these sections correlate the assumed linear power capabilities of the receiver components with the S/N matrices.

The succeeding sections of the report include the tracking loop design, AGC loop design and detailed mechanization data of each receiver unit. In conclusion the receiver specification is compared with the exceptions listed.

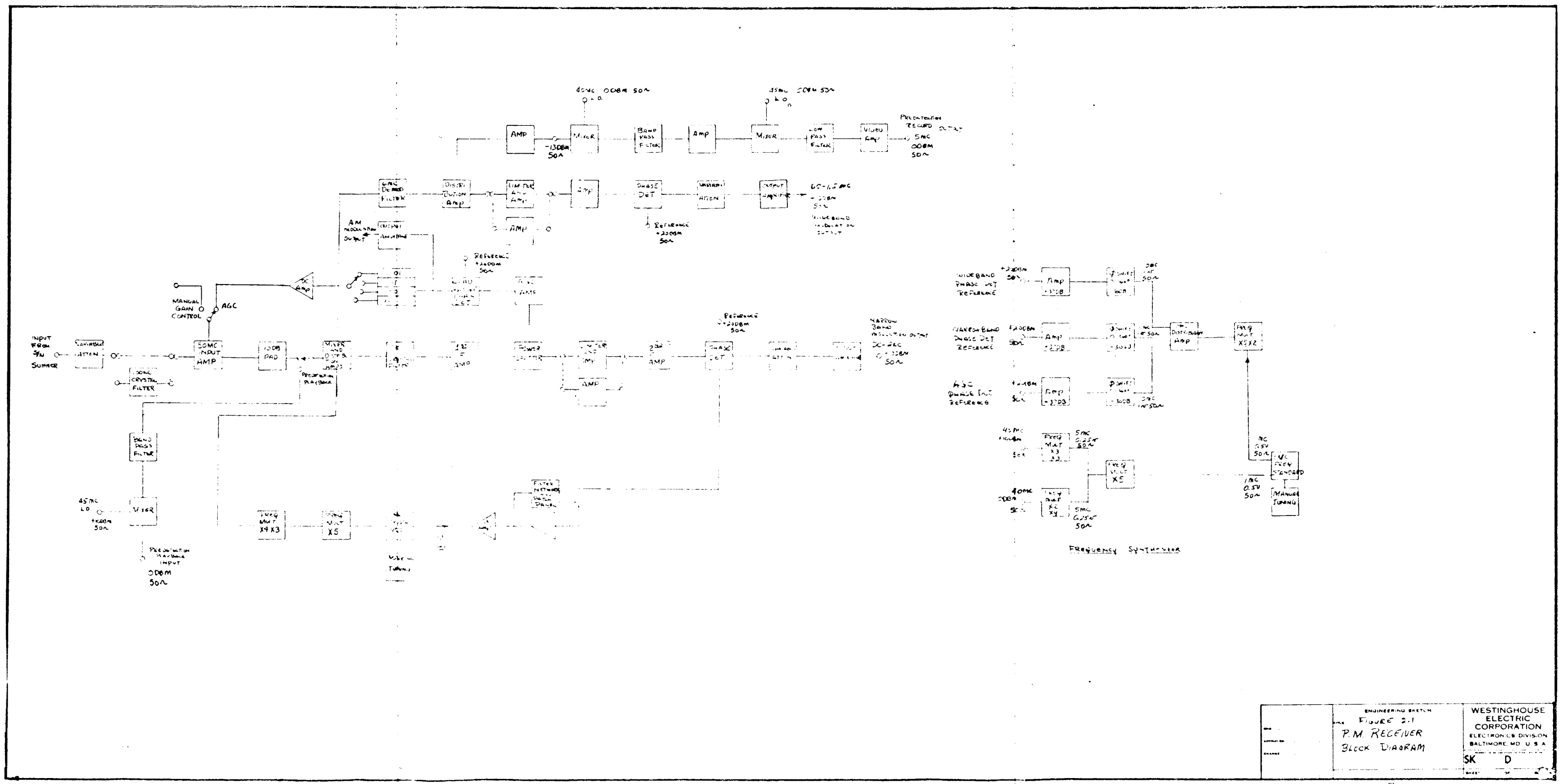
2.1 P.M. Receiver Block Diagram

Figure 2.1 indicates the PM receiver block diagram. The basic configuration is essentially the same as outlined in JPL Spec. SSD-10002-DRN. The changes are listed below. The detailed reasons for the changes are included in the appropriate succeeding sections.

1. A variable attenuator (0-35 DB) precedes the Input Amplifier.

2. Provision is made to substitute a 100 KC filter prior to the Input Amplifier.

3. The 10 mc reference oscillator shall be mechanized as a 1 mc oscillator with appropriate frequency multipliers.



	ENGINEERING SKETCH FIGURE 2-1 P.M. RECEIVER BLOCK DIAGRAM	WESTINGHOUSE ELECTRIC CORPORATION ELECTRONICS DIVISION BALTIMORE, MD. U.S.A. SK D

4. The 60 mc VCO shall be mechanized as a 1 mc oscillator with appropriate frequency multipliers.

5. The predetection record mechanization shall include an additional stage of up and down conversion.

6. The predetection playback shall include an additional stage of up conversion.

2.2 S/N Summer Matrices

The signal to noise ratio capability of the S/N Summer is shown in matrix form in figure 2.2. Consider figure 2.2A. The matrix is referenced to a noise bandwidth of 3.0 cps (2BLO = 3.0 cps). Par. 3.5.1.3.8 specifies that the minimum standard loop noise bandwidth shall be 3.0 cps defined at the receiver absolute threshold (0db S/N ratio in 2BLO). However, the loop noise bandwidth must be variable from 1 to 1000 cps at differently defined thresholds. As shown by matrix 2.2A, 0db S/N is achieved at the signal and noise levels of -70 dbm. The S/N Summer Signal and Noise attenuator's range extend from 0db to 61db although the matrix indicates 0db to 50db. Therefore, if required, the minimum signal level can be ex-

S/N

NOISE BW 3dB

FIGURE 2.2.9

	ENGINEERING SKETCH FIGURE 2.2 S/N SUMMER S/N RATIO AS A FUNCTION OF NOISE BANDWIDTH	WESTINGHOUSE ELECTRIC CORPORATION ELECTRONICS DIVISION BALTIMORE, MD. U.S.A. SK. B SHEET OF SHEETS

tended to -81dbm yielding a S/N of -11db in a noise bandwidth of 3.0 cps.

The S/N ratios referenced to 2KC, 6 mc and 10 mc noise bandwidths are shown in Figures 2.2B, 2.2C and 2.2D respectively.

2.3 Tracking Loop Signal and Noise Power Levels

Figure 2.3 indicates the PM Receiver Carrier Tracking channel signal and power levels over the dynamic range of the S/N Summer. Row 1 shows the gain (or loss) of each channel component drawn in the block diagram found in figure 2.3. Rows 2 through 9 indicate various input signal and noise levels. Columns 4 through 21 indicate the signal and noise levels at the block diagram components for the assumed input signal and noise levels. Consider Row 2. The minimum unmodulated carrier signal is -70db, the noise is zero. Tracing across row 2, the attenuator loss is 0db and the signal level at the input amplifier is -70dbm. The Input Amplifier gain is +16db; therefore, the signal level to the 10db pad is -54dbm etc. Tracing across row 2 to column 22, note that the power input to the phase detector is 20dbm and the limiter is in 6db of limiting on the unmodulated carrier. The limiter output limit level is 0dbm as shown in column 20.

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The RMS output power capability of each component in the block diagram is listed in row 10. The block diagram components are linear to 3σ. For example, the 1st IF output RMS linearity is listed as 0dbm. The unit shall be linear to + 10dbm (3σ). To examine any block diagram component for overload for various signal and noise power inputs compare row 10 with the signal and noise power listed.

The S/N Matrices Figures 2.2A through 2.2D list the minimum unmodulated carrier as -70dbm. Row 2, column 7 of Figure 2.3 indicates that the AGC regulates the Input Amplifier gain at 16db on the minimum carrier. Row 3, column 7 shows that when the carrier is suppressed 11db by modulation the Input Amplifier gain is maximum and the receiver is at AGC Threshold. Therefore, the maximum allotted carrier suppression attributed to modulation is 11db.

Figure 2.1, the PM Receiver Block Diagram, lists a variable attenuator prior to the Input Amplifier. The S/N Matrices, Figure 2.2, indicate the signal dynamic range as -20dbm to -70dbm. An additional 11db carrier dynamic range is attributed to angle modulation. The total carrier dynamic range is 61db. If the Input Amplifier and AGC system are designed to accommodate

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64db variation of carrier level, the Input Amplifier gain must be at least 64db. However, as will be pointed out later in this section the receiver gain at 10 mc bandwidth must be minimized. Therefore, the dynamic range of the Input Amplifier gain has been established as 30db or 14db to accommodate change in carrier level attributed to angle modulation and 16db to accommodate carrier level changes made in the S/N Summer. The input Variable Attenuator range extends from 0 to 35db. The total receiver carrier dynamic range is 65db - 30db AGC and 35db manual.

The S/N Matrices, Figure 2.2A and 2.2D show the relative S/N ratios as a function of the 10 mc receiver front end noise bandwidth and the 3 cps minimum tracking loop absolute threshold noise bandwidth. It is imperative that the tracking loop be tested at 3 cps 2 BLO. However, what happens to the 10 mc bandwidth front end at this S/N ratio? Figure 2.2D, Row 1, column 6 indicates the S/N ratio is -65.24 dbm in 10 mc when the S/N ratio in 3 cps is 0dbm as shown by Figure 2.2A row 1 column 6. The PM Receiver Tracking channel Level Diagram, Figure 2.3, Row 5 shows the relative signal and noise power levels throughout the receiver front end and tracking loop for 0db S/N in 2 BLO of 3 cps. A comparison of row

B

5 and row 10, Figure 2.3, indicates that the Input Amplifier and Mixer are overloaded on noise by 11.24 dbm and +4.24 dbm respectively. The problem is attributed to the large difference of noise bandwidth of the receiver front end and carrier tracking channel. The problem would become more difficult if the Input Amplifier gain were increased to accommodate the 64db carrier dynamic range with the AGC system.

One solution, is to build the receiver front end (Input Amplifier and Mixer) such that noise overload doesn't occur at S/N of -65.24db in 10 mc. The linear peak power capability of the Input Amplifier and mixer must become +21.24dbm and +14.24dbm respectively (allowing 10dbm of linear power capability above RMS noise). However, the S/N ratio at the wideband demodulation channel phase detector is -63db (6mc noise bandwidth) under these conditions. The resulting data from the demodulation channel is of doubtful value at -63db S/N ratio. Further, the task of building the Input Amplifier and Mixer to accommodate the noise levels quoted, in our opinion, is not practical. An alternate solution is to provide a 100 KC noise bandwidth filter prior to the Input Amplifier when testing the tracking loop for

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Odb S/N in 2 BLO of 3.0 cps. The resulting signal and noise power levels in 100 KC noise bandwidth throughout the receiver front end and carrier tracking channel are indicated by figure 2.3 row 6. A comparison of row 6 and row 10 reveals that the 100 KC filter preceding the receiver front end reduces the noise power to an acceptable level (mixer 1.24 db overload).

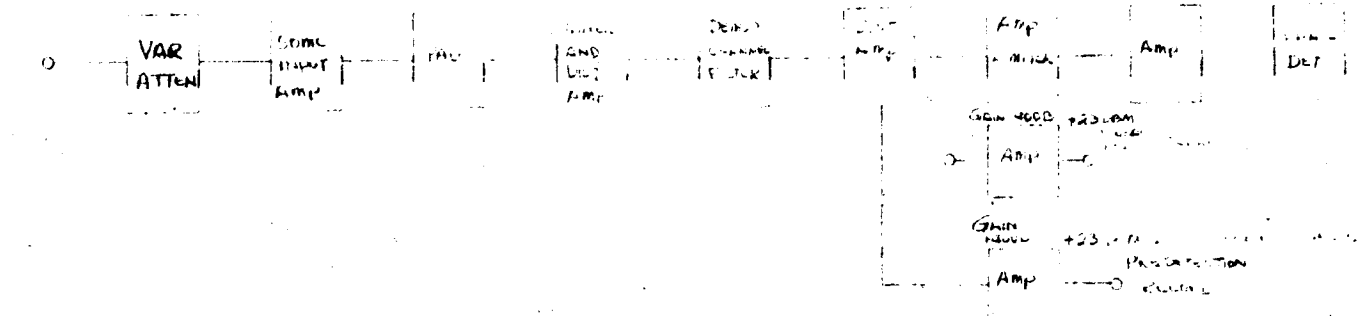
The RMS power capability of each unit in the receiver front end and the predetection portion of the tracking loop is listed in row 10 figure 2.3. The second IF amplifier shall be capable of delivering 2 watts linear, small signal power (+33 dbm). The RMS linear capability is listed as +23 dbm allowing an additional 10dbm linear capability. The same criteria has been applied to all the power capabilities listed in row 10 figure 2.3.

2.4 Demodulation Channel Signal and Noise Power Levels

Figure 2.4 constitutes a matrix correlating input signal and noise levels with the receiver front end and wideband demodulator power capabilities. The diagram displays the same data as figure 2.3 but figure 2.4 is referenced to the receiver front end and wideband demodulation channel.

Rows 1, 2 and 3 of Figure 2.4 indicate the dynamic range of all wide-

1	2	3	4	5	6	7	8	9															
			GAIN IN DB →		(-35)			(+30-0)		-10		+3		-3		+4		(60-0)		1 KC		S/N IN MEGACYCLE BW	
1	RMS SIGNAL	RMS NOISE	MINIMUM UNMODULATED CARRIER	-70DBM	(0)	-70DBM		(+16)		-54DBM	+10	-54DBM	+3	-57DBM	-3	-64DBM	+4	-60DBM	4 WAY	0DBM	+20	+20DBM	
2	RMS SIGNAL	RMS NOISE	MINIMUM MODULATED CARRIER	-84DBM	(0)	-84DBM		(+30)		-54DBM	-10	-67DBM	+3	-67DBM	-3	-64DBM	+4	-60DBM	+60	0DBM	+20	+20DBM	
3	RMS SIGNAL	RMS NOISE	MAXIMUM UNMODULATED CARRIER	-20DBM	(-34)	-54DBM		(0)		-54DBM	(-0)	-64DBM	+3	-64DBM	-3	-64DBM	+4	-60DBM	(+60)	0DBM	(+20)	+20DBM	
4	RMS SIGNAL	RMS NOISE	MINIMUM UNMODULATED CARRIER MAXIMUM NOISE	-70DBM -47.6DBM	(0)	-70DBM -47.6DBM		(+16)		-54DBM +11.24DBM	+16	-64DBM +9.24DBM	+3	-64DBM +9.24DBM	-3	-64DBM -14.76DBM	+4	-60DBM +4DBM	(0)	0DBM	(+20)	20DBM	-40DB
5	RMS SIGNAL	RMS NOISE	UNMODULATED CARRIER NOISE	-50DBM -87.6DBM	(-4)	-54DBM -127.6DBM		(0)		-54DBM -127.6DBM	(-0)	-67.6DBM -22.76DBM	+3	-67.6DBM -22.76DBM	-3	-67.6DBM -24DBM	+4	-60DBM -20DBM	(+30)	0DBM	(+20)	20DBM	-40DB
6																							
7																							
8																							
9	NOISE BANDWIDTH								10MC					6MC									
10	RMS POWER CAPACITY LINEAR TO 3T								0DBM			-11DBM				0DBM		0DBM		+23DBM			



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P.M. RECEIVER

DEMODULATION CHANNEL

LEVEL DIAGRAM

FIGURE 2.4

band demodulation channel components shown in the block diagram at the bottom of the figure as the noise free carrier is varied from -20dbm to -84dbm. Row 4 indicates the noise overloading for a S/N ratio of -65.24 db in 10 mc or -63db in 6 mc. If uncontrolled limiting (noise overloading) occurs at a S/N ratio of -63db in the 6 mc demodulation bandwidth, what S/N ratio should the demodulation channel accommodate? The cognizant engineer has suggested that the S/N ratios of principal interest extends from 0db to -30db in the 6 mc bandwidth. A S/N ratio of -40db in the 6 mc bandwidth is listed in row 5, figure 2.4. As shown the mixer is close to noise overload; however, the other components are below the maximum allotted power capacity. Therefore, a S/N ratio of -40db in 6 mc noise bandwidth is specified as the limit of the wideband demodulator channel. Numerically this means that the wideband demodulation channel shall operate with controlled limiting at any point on the figure 2.2C and 2.2D matrix below the lines indicated. Further, this means that the ratios of RMS noise voltage to RMS signal voltage at the video output of the wideband phase detector shall be 100/1.

3.0 Carrier Tracking Loop Design

3.1 Limiter Suppression

Paragraph 3.5.1.3.8 b states: "The receiver shall have (4) standard loop noise bandwidths of 3, 12, 20 and 48 cps in the passive configuration defined at the receiver absolute threshold operating point. It shall be possible to simply and reliably change the loop filter components in order to operate with either the same bandwidths at different threshold points, or with any other loop noise bandwidth from 1 to 1000 cps".

Consider the selection of 2 BLO = 1.0 cps. The S/N ratio in the loop noise bandwidth at the receiver absolute threshold is assumed to be 0db. The predetection noise bandwidth is 2 KC as established by the narrow band IF amplifier. The S/N ratio in the predetection bandwidth is simply the ratio of loop noise bandwidth to predetection bandwidth or 10 Log 1/2000 = -33db. It is assumed that modulation components in the predetection bandwidth do not add to the noise power. The suppression factor of the tracking loop limiter, α_o, as outlined by Martin[1] is:

$$\alpha_o^2 = \frac{1}{1 + \frac{4}{\pi}\left(\frac{N}{S}\right)_i} \qquad (1)$$

Since N/S = 2000/1, α_o = .02. The limiter suppression factor above threshold, α, approaches unity as a limit. The ratio of limiter suppression factor at threshold to that above threshold becomes $\frac{\alpha_o}{\alpha} = .02 = \mu$.

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3.2 Tracking Loop Parameters at Threshold

The specification indicates (par 3.5.1.3.7) that the PM receiver loop gain shall be sufficiently large such that the residual loop static phase error is negligible over the normal receiver operating range as determined by the transmitter tuning range and the system frequency instabilities, when the VCO is tuned to its zero-voltage quiescent frequency. The loop gain stability over this same range shall be within $\pm$ 3 percent of nominal.

The relationship between loop gain and residual phase error is indicated by equation 2.

$$\Delta\Omega = \frac{K\,\Delta\omega}{S} \qquad (2)$$

where $\Delta\omega$ represents the detuning of the transmitter standard (500 cps) plus the long term instabilities of the transmitter/receiver frequency standards. Assume the specified negligible phase error is assigned the value of one degree. Further, assume that the specified negligible residual phase error is meaningful only above threshold. The no noise loop gain (G) required is

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$$G\left(\frac{1}{sec}\right) = \frac{500 \text{ cps} \cdot 360 \text{ °/cycle}}{1 \text{ deg.}} = 180{,}000 \quad (3)$$
$$= 105 \text{ db}.$$

The specification sug ests that the tracking loop design optimize the loop at threshold. Therefore, the no-noise loop gain G ($2\pi K_m K_{VCO} K_a$) is modified to include the limiter suppression as follows: $G_o = 2\pi K_m K_{VCO} K_a \alpha_o$ = 180,000 . 0.02 = 3600 $\frac{1}{\text{sec.}}$ The basic loop relationships as outlined by Martin, Rechtin and ...affe include:

$$\frac{e_o(s)}{e_i(s)} = \frac{1 + \tau_2 s}{\tau_1 s} \quad (4)$$

$$\tau_1 = (K_1 + K_2) C = \frac{G_o}{B_o^2} \quad (5)$$

$$\tau_2 = K_2 C = \frac{2\zeta}{B_o} \quad (6)$$

$$\zeta_o = \frac{1}{\sqrt{2}}$$

$$2B_{L_o}(cps) = 1.04 B_o(rps) = 6.55 f_o(cps) \quad (7)$$

It follows that for 2BLO = 3.0, 12.0, 20.0 and 48.0 cps with Go = 3600 1/sec the time constants τ_1 and τ_2 become as listed in Table 3.1.

$2B_{LO}$	τ_1 (Sec)	τ_2 (Sec)	G_o (1/sec)
3.0	450	0.5	3600
12.0	12.0	0.125	3600
20.0	10.05	0.075	3600
48.0	1.75	0.031	3600

Table 3.1 Loop Time Constants

3.3 Tracking Loop Parameters Above Threshold

The tracking loop is optimized with regard to noise bandwidth at threshold. Above threshold the limiter suppression factor, α, approaches unity as the limit. The loop gain, damping, natural resonant frequency and noise bandwidth vary as outlined by

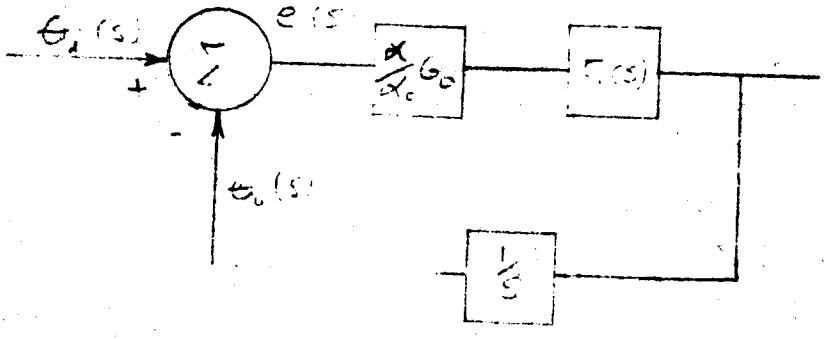

Figure 3.1 Linear Phase Model, APC Loop Above Threshold

Equations (4), (5), and (6) on page 16.

above threshold G_0 becomes $\alpha/\alpha_0 G_0$

$$F_1(s) = \frac{\sqrt{2}/B_0 s + 1}{G_0/B_0^2 s} = \frac{B_0^2(1 + \sqrt{2}/B_0 s)}{G_0 s} \quad (11)$$

$$H_0(s) = \frac{\alpha}{\alpha_0} \frac{G_0}{s} F_1(s) = \frac{\alpha}{\alpha_0} \frac{B_0^2 (1 + \sqrt{2}/B_0 s)}{s^2} \quad (12)$$

$$H(s) = \frac{H_0(s)}{1 + H_0(s)} = \frac{\frac{\alpha}{\alpha_0} \frac{B_0^2 (1 + \sqrt{2}/B_0 s)}{s^2}}{1 + \frac{\alpha/\alpha_0 B_0^2 (1 + \sqrt{2}/B_0 s)}{s^2}} \quad (13)$$

$$H(s) = \frac{\Theta_0(s)}{\Theta_i(s)} = \frac{1 + \sqrt{2}/B_0 s}{\frac{\alpha_0}{\alpha} \frac{s^2}{B_0^2} + \frac{\sqrt{2}}{B_0} s + 1} \quad (14)$$

pf

$$1 - H(s) \equiv \frac{e(s)}{\theta_i(s)} = 1 - \frac{1 + \frac{\sqrt{2}}{B_0} s}{\frac{\alpha_0}{\alpha}\frac{s^2}{B_0^2} + \frac{\sqrt{2}}{B_0} s + 1} \tag{15}$$

$$1 - H(s) = \frac{e(s)}{\theta_i(s)} = \frac{\frac{\alpha_0}{\alpha}\frac{s^2}{B_0^2}}{\frac{\alpha_0}{\alpha}\frac{s^2}{B_0^2} + \sqrt{2}\frac{s}{B_0} + 1} \tag{16}$$

$$\omega_n = \sqrt{\frac{\alpha}{\alpha_0}}\, B_0 \tag{17}$$

$$\zeta = \sqrt{\frac{\alpha}{\alpha_0}} \cdot 0.707 \tag{18}$$

$$2B_L = \frac{2B_{L0}}{3}\left(1 + 2\frac{\alpha}{\alpha_0}\right) \tag{19}$$

The influence of α/α_0 on the closed loop response $H(s)$ is indicated as follows from equation (14):

$$|H(s)| = \left[\frac{1 + 2\left(\frac{\omega}{B_0}\right)^2}{\left\{1 - \frac{\alpha_0}{\alpha}\left(\frac{\omega}{B_0}\right)^2\right\}^2 + 2\left(\frac{\omega}{B_0}\right)^2}\right]^{1/2}_{s=j\omega} \tag{21}$$

The plot of H (s) as a function of ω/B_o at threshold and above threshold is indicated in figure 3.2. It follows that the influence of α/α_o on 1-H(S) is similarly computed from equation (16).

$$\left|1 - H(s)\right| = \frac{\alpha_o/\alpha \left(\frac{\omega}{B}\right)}{\left[\left[1 - \frac{\alpha_o}{\alpha}\left(\frac{\omega}{B}\right)\right]^2 + 2\left(\frac{\omega}{B_o}\right)^2\right]^{1/2}} \Bigg|_{s=j\omega} \quad (23)$$

The plot of $1 - H(s)$ as a function ω/B_o is also indicated in figure 3.2. Table 3.2 summarizes the effects of limiter suppression on the 1.0 cps noise bandwidth loop.

	Threshold	Above Threshold
2BLO	1.0 cps	33.7 cps
Wn	0.994 rad/sec	6.67 rad/sec
ζ	0.707	5.0
α	0.02	1

$$H(s) \quad \frac{\left(1 + \sqrt{2}/B_o s\right)}{1 + \sqrt{2}/B_o s + \zeta^2/B_o^2} \quad \frac{\left(1 + \sqrt{2}/B_o s\right)}{1 + \frac{\sqrt{2}}{B_o} s + \frac{\alpha}{\alpha}\frac{\zeta^2}{B_o^2}}$$

$1 - H(s)$

Table 3.2 Summary of Limiter Suppression

Table 3.3 indicates the influence of on the various loop configurations

2BLO	2BL		
1.0 cps	33.7 cps	6.67 rad/sec	50
3.0	59	15.2	29
12.0	120.8	43.3	14.6
20.0	157	63.	11.3
48.0	251	123	7.36
1000.0	1580	1290	1.87

Table 3.3 Effects of Limiter Suppression on Specified Tracking Loop Bandwidths.

3.4 Tracking Loop Filters

The carrier tracking loop filter can be mechanized either with passive components or an active operational amplifier in association with passive

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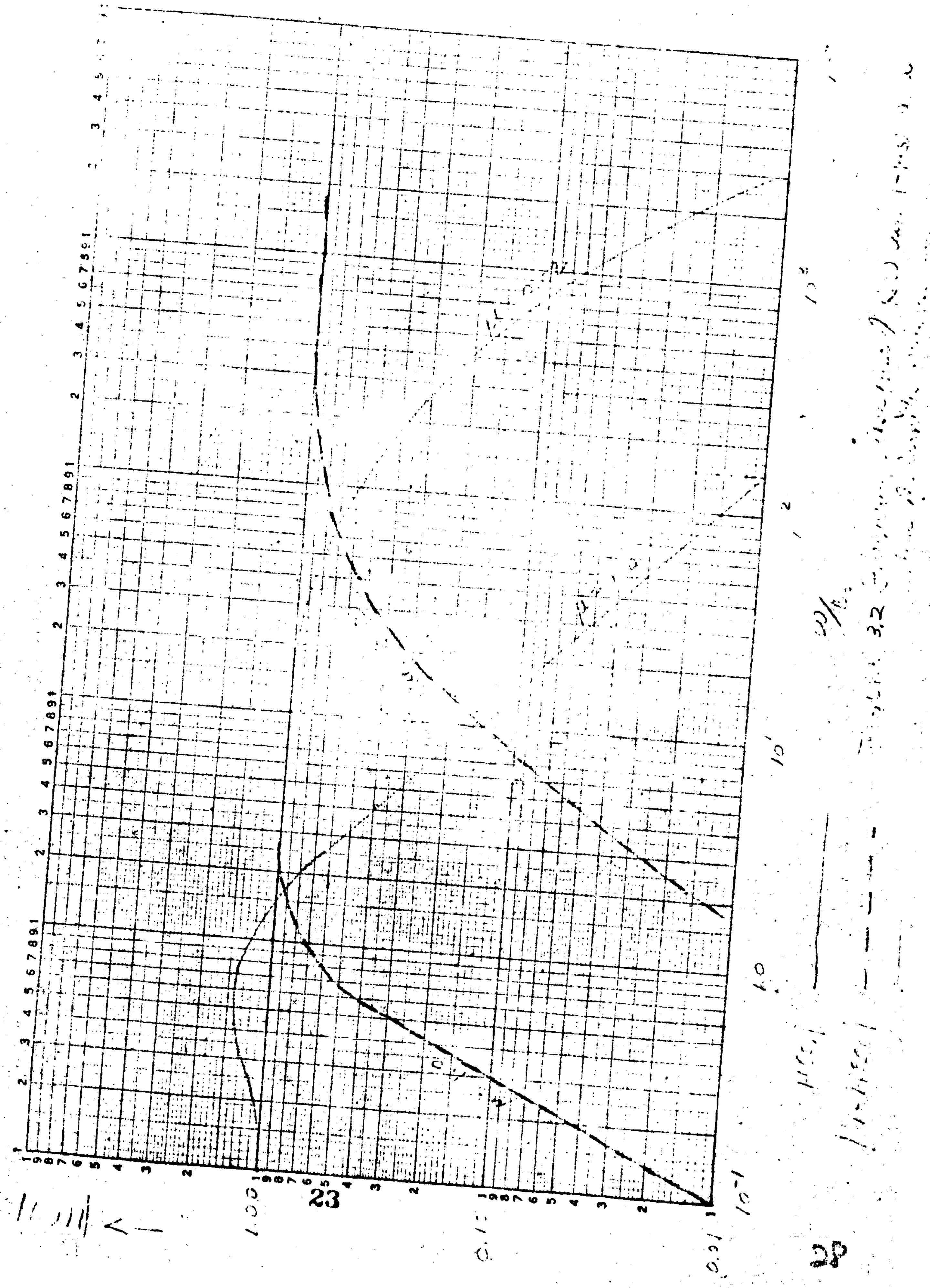

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components. Each approach has its advantages and its limitations as discussed below.

The passive circuit is of the familiar form shown in Figure 3.3.

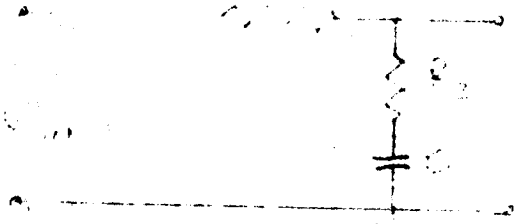

Figure 3.3 Passive Filter

This lag-lead network has the advantage of simplicity and stability with the use of precision resistors and capacitors. The disadvantages become apparent in applications requiring large time constants.

For example, for a desired bandwidth of 1 cps ($2 B_{LO}$) and an open loop gain of 360 1/sec the value of $\tau_1 = (R_1 + R_2) C$ is equal to where $B_o = 2 B_{LO}/1.06$. τ_1 = 404 seconds and the value of R_1 is 40.25 megohms. This order of resistance requires special consideration with regard to class of component and mounting. A leakage path from terminal to terminals should be of 40,000 megohms or higher.

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A more severe leakage problem occurs in the amplifier circuit following the filter time constants. Depending on the approach taken the resistances encountered in such a circuit could be in the range of thousands of megohms and leakage requirements near the million megohm level.

By taking special precautions in the design of these low leakage circuits the desired values can be achieved. Glass sealed resistors are available to values of millions of megohms. For high resistance in operational amplifier applications one approach which has been proven to be effective provides a grounded strap mounting which diverts surface leakage currents to ground while preserving a high terminal resistance. For mounting on a printed circuit card it is necessary to use a clad material which has very low moisture absorption such as teflon. The use of ground separation between terminals and dust proof containers are also helpful.

Although the above methods can be applied to solve many leakage problems it remains difficult to insure that a desired tolerance of 1%

will be maintained under various environmental conditions. It is desirable to restrict the resistance values, if possible, to those which are not excessive where more standard, less expensive components and techniques can be employed.

It should be noted that the leakage problem becomes less severe as the loop bandwidth is widened. For the higher bandwidths the passive filter can be applied without reservation. For the low bandwidths a more satisfactory approach would use the active filter including an operational amplifier. Actually in both the active and passive filters an amplifier is required. The passive filter requires an isolating amplifier to properly load the passive circuit.

The active filter will take the form shown in Figure 3.4.

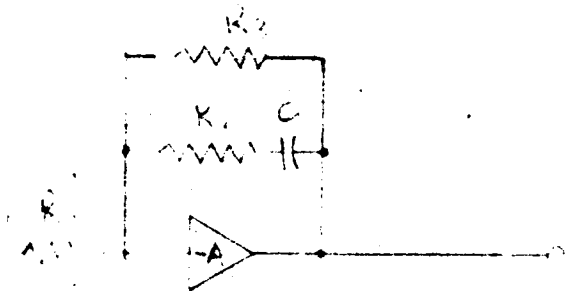

Figure 3.4 Active Loop Filter

The circuit consists of a high gain dc amplifier with input and feedback networks to achieve a lag-lead response identical to the passive filter. Ideally, the lag corner would not be necessary to loop operation. However, amplifiers are never completely free of drift and the dc feedback resulting from R_3 prevents the amplifier from drifting to saturation when the loop is unlocked for prolonged intervals.

The active filter has the distinct advantage of a relatively low output impedance such that the circuitry which follows will not load the filter and degrade its performance. The filter will be arranged to have a slight loss of 3.5db by making $R_1 = 1.5\ R_3$. The reason for this is to prevent overload on low frequency beats which occur when the loop is unlocked and which will reach an amplitude of $\pm$ 15 volts pp. Since the amplifier is rated for only $\pm$ 10 volts pp it is desirable to take the small loss in order to keep the filter linear.

Four bandwidths ($2\ B_{LO}$ = 3, 12, 20 or 48 cps) will be selectable for the carrier tracking loop by a flexible patching arrangement which connect the required components for the passive filter or for the input

and feedback networks of the active filter. The internal 10 μfd capacitor will remain fixed for all bandwidths provided internally. External filter arrangements can be applied via appropriate terminals at the patch panel. For each of the four bandwidths the dc gain and lag corner can be selected to permit a 30 degree phase error in the presence of a 500 cps frequency error. Since the phase error would normally be 1 degree, in order to cause a 30 degree error the loop gain must be reduced and the lag corner suitably corrected.

Table 3.4 is a summary of the loop filter parameters and component values for the passive filter shown in Figure 3.5. The values shown are also applicable to the passive filter indicated in Figure 3.6.

For both filter configurations the circuit components must be high quality precision units. The resistors will normally be carbon deposited, 1%, resistors of the RN70B class. Victorean glass sealed resistors will

be used for the higher resistance values.

The capacitor used must exhibit very high insulation resistance with a capacitance tolerance of 3% or better. The insulation resistance must be at least 1000 times the highest value of R_2 in order to degrade R_2 by no more than .1%. Plastic film capacitors with dielectrics of mylar, polystyrene, or teflon are commonly used in such applications. Mylar capacitors have insulation resistance times capacitance values of 10^5 megohm-ufarads at 25°C. The 10 ufd unit therefore has an insulation resistance of 10^4 megohms. The highest value of R_3 in table 3.4 is 4.03 megohms, therefore, the mylar unit is suitable. The other dielectrics mentioned have insulation resistance values greater than mylar and consequently are also suitable. The mylar unit will be physically smaller than polystyrene or teflon capacitors and therefore is preferred.

The operational amplifier considered is the Philbrick SP456 chopper stablized unit. The manufacturer states that this amplifier can be connected to provide a dc input resistance of 1 million megohms. Such an amplifier will be suitable in the active filter as well as the follower

amplifier for the passive filter. The low drift, low noise, and wide bandwidth make this amplifier suitable for most of the operational amplifier applications in the receiver.

Following the filter network, including the isolating amplifier for the passive filter, is a second operational amplifier (SP 456) arranged for a maximum gain of 35.8 db. Summed at the input of this amplifier is a variable dc current which will serve as a VCO frequency control during acquisition and open loop testing.

A switch will be provided to ground the VCO input to permit setting the VCO quiescent frequency.

SKETCH SHEET
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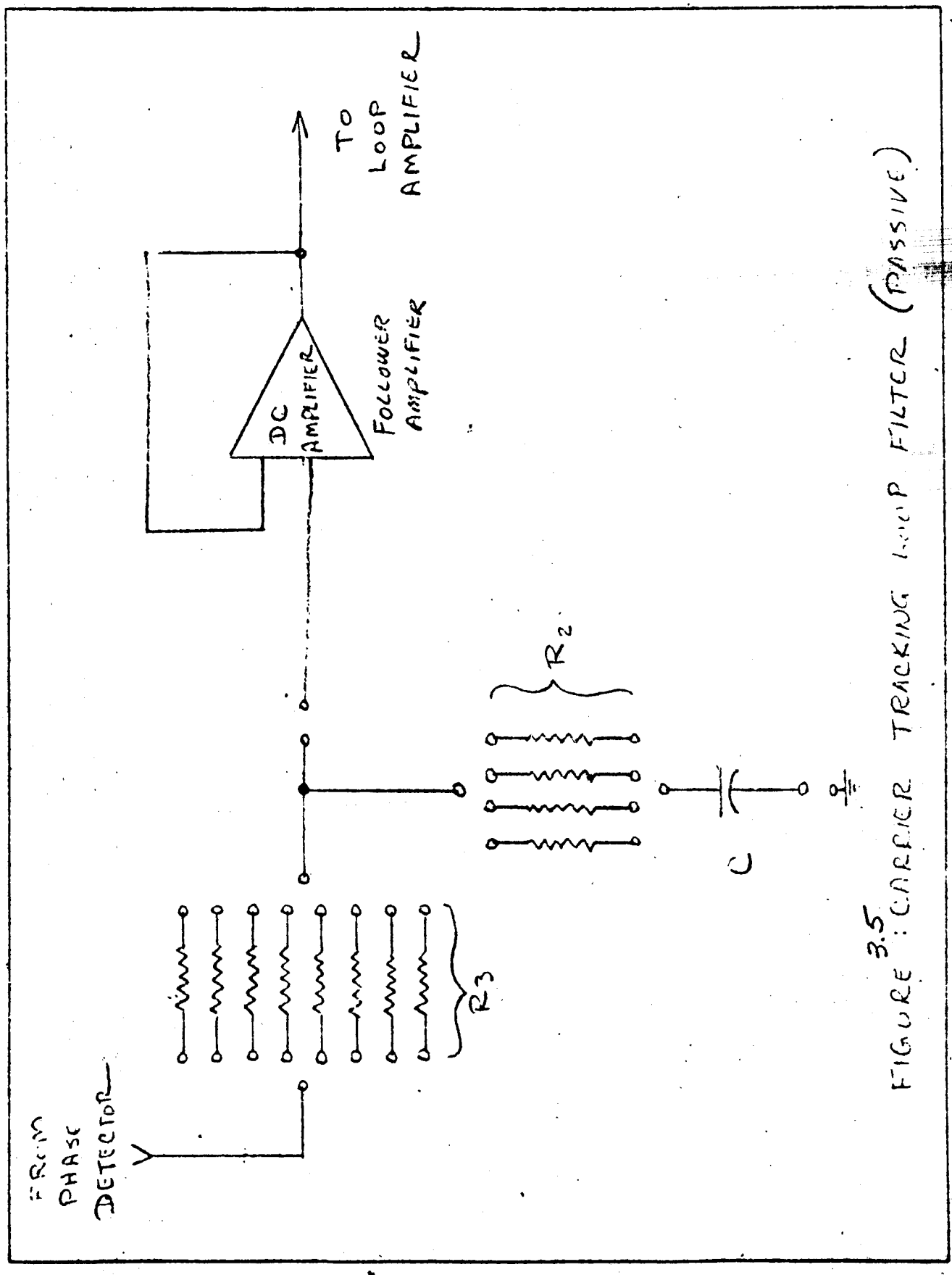

FIGURE 3.5: CARRIER TRACKING LOOP FILTER (PASSIVE)

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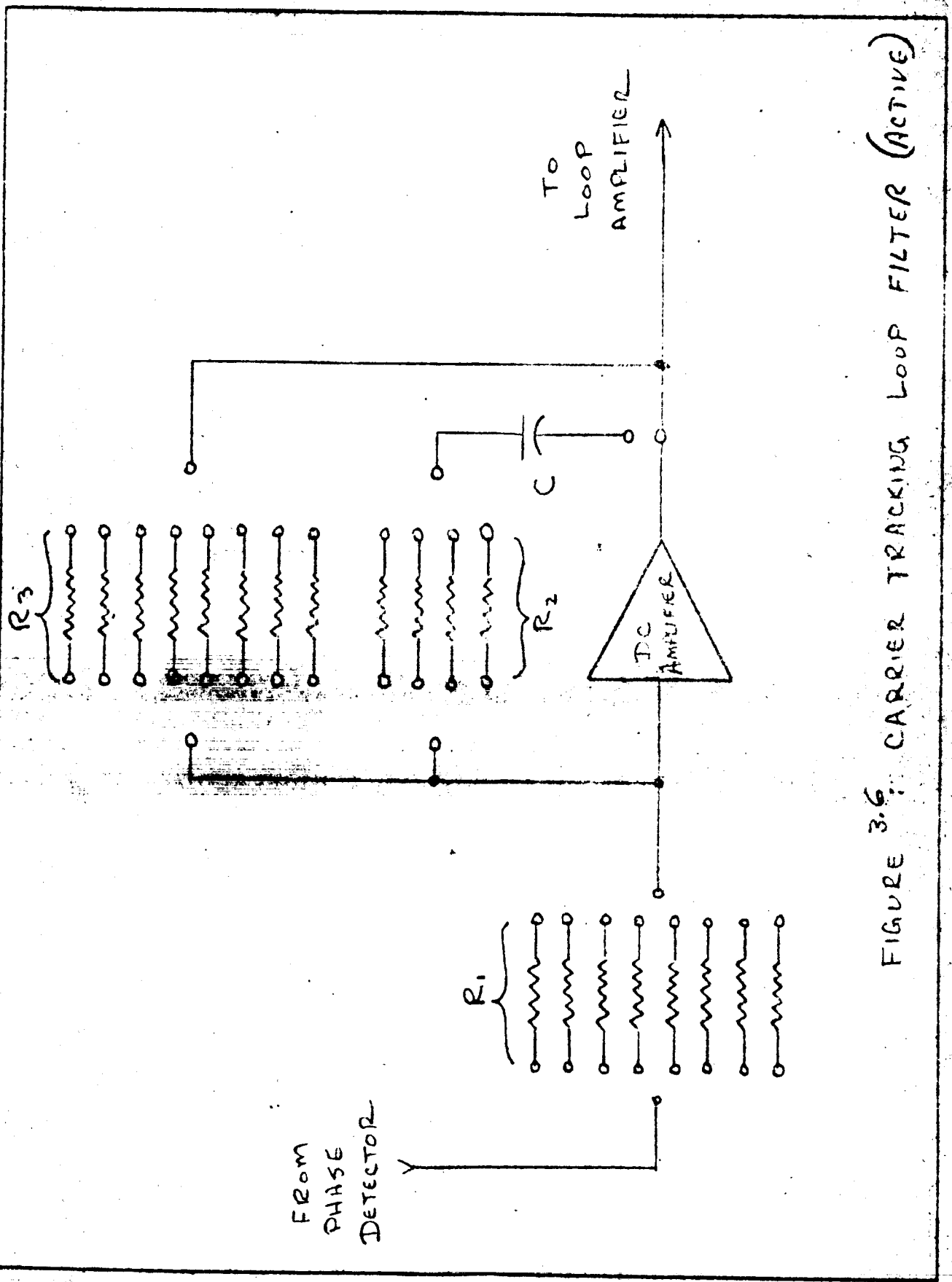

FIGURE 3.6 CARRIER TRACKING LOOP FILTER (ACTIVE)

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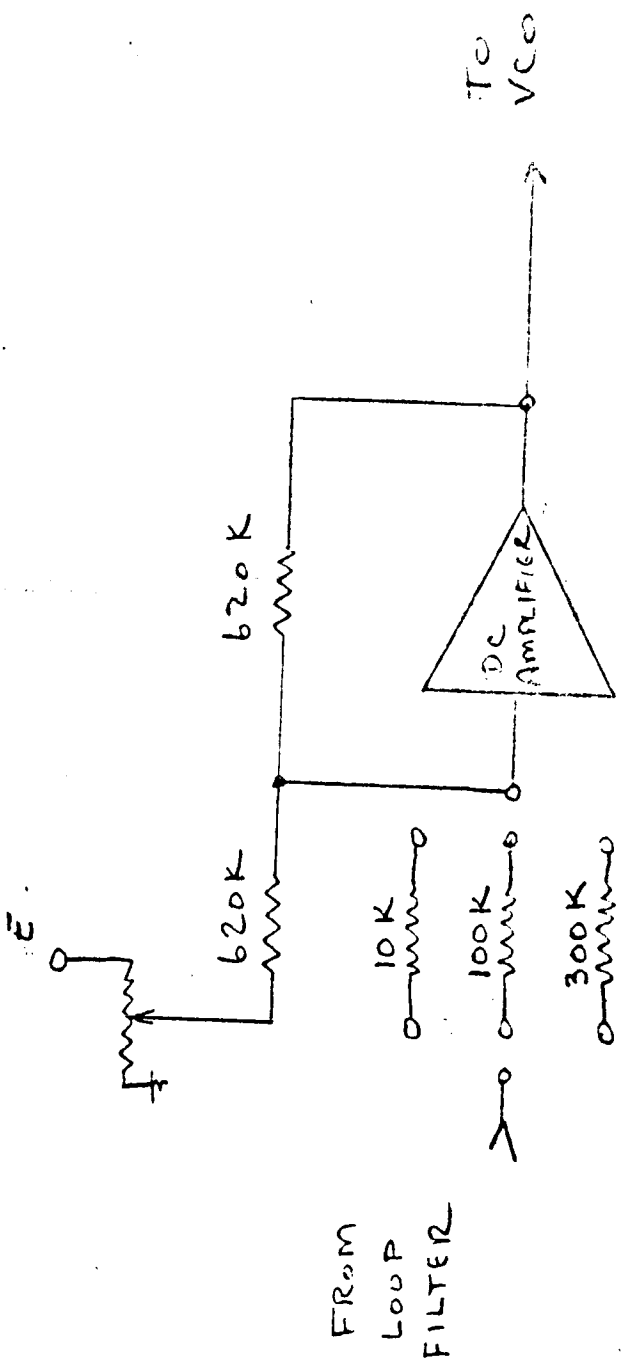

DC GAINS = 35.8, 15.8, OR 6.3 DB

FIGURE 3.7 CARRIER TRACKING LOOP AMPLIFIER

TABLE 3.4: CARRIER TRACKING LOOP
PARAMETER & COMPONENT VALUES

See P27

$2B_{LO}$ CPS	B_o RAD/SEC	G_o 1/SEC	T_1 SEC	T_2 SEC	R_1 mΩ	R_2 mΩ	R_3 mΩ	C MFD
3	2.83	3600	450	0.5	6.68	.05	445	100
3	2.83	120	15	0.5	2.18	.05	145	10
12	11.3	3600	28.2	0.125	422	.0125	2.81	10
12	11.3	120	9.4	0.125	1.39	.0125	.928	10
20	18.9	3600	10.05	0.075	1.5	.0075	.998	10
20	18.9	120	3.35	0.075	.492	.0075	.328	10
48	45.3	3600	1.75	0.031	.257	.0031	.172	10
48	45.3	120	.58	0.031	.083	.0031	.055	10
1	0.943	3600	404	1.5	60.4	.15	40.25	10
1	0.943	3600	404	1.5	6.04	.015	4.025	100
1000	943.0	3600	.0404	.0015	.0382	.015	.0254	0.1

4.0 TRACKING LOOP MECHANIZATION.

4.1 DISTRIBUTION OF TRACKING LOOP GAIN

This section of the study deals with the correlation between tracking loop equations and the tracking loop hardware. Consider the open loop gain at threshold, Go, and above threshold, G. The above threshold open loop gain must be 180,000 to constrain the residual phase to one degree when the transmitter carrier is detuned 500 cps. The open loop gain above threshold is expressed by equation 24.

$$G\ (\text{sec}^{-1}) = 2\pi (K_m K_{vco} K_a K_x) \qquad (24)$$

K_m is the phase detector sensitivity in $\frac{\text{volts}}{\text{radian}}$, Kvco the VCO sensitivity in $\frac{\text{cycles}}{\text{volt sec.}}$, Ka the D.C. amplifier gain in volts/volt and Kx the frequency multiplication factor in $\frac{\text{cps}}{\text{cps}}$. The latter constant in this instance is 60 (1mc multiplied to 60 mc). Therefore, Km Kvco Ka = $\frac{180,000}{60(2-)}$ = 478. The wideband phase demodulator developed for the data demodulation channel exhibits a linear voltage transfer of video output to signal input of 40 volts peak to peak. If 75% of the unit's peak capability is used, Km be-

comes $\frac{15 \text{ volts}}{\text{radian}}$. The remainder of the required gain is divided between the VCO and D. C. amplifier. A suitable value of Kvco is 1.0 $\frac{\text{cycle}}{\text{volt sec.}}$ Thus Ka, the loop amplifier gain, becomes 32.

The loop gain contribution of the remaining loop components; namely, the Balanced Modulator, Crystal Filter, 10mc IF amplifier and limiter are included in Km, the phase detector constant. Further, noise threshold Km is diminished by the factor A/σ_n and [illegible]. The loop gain factors Ka and Kvco are constant either above or at threshold within the constraints of the linearity of the DC amplifier and VCO. The multiplier constant, Km varies from $\frac{15 \text{ volts}}{\text{radian}}$ to 0.3 $\frac{\text{volts}}{\text{radian}}$ at threshold.

Ideally $F_1(s)$ contributes all the meaningful loop corners. In a practical sense the loop D.C. amplifier will contribute a loop corner at its 3DB amplitude response. However, this corner will occur at a frequency sufficiently far removed from the principal loop time constants and will be of little concern. However, the specification indicates that the loop noise bandwidth may extend to 1000 cps (fo = 151 cps). The loop amplifier shall corner at least two decades above 150 cps. However, the 2KC crystal filter is another matter.

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This unit is inside the tracking loop and its amplitude and phase response must be considered in the loop mechanization. The crystal filter contributes a complex pole at 1000 cps.

Another subtle loop corner is contributed by the VCO. The VCO transfer function is usually expressed as $Kvco/_s$. However, in reality the transfer function is $\frac{Kvco}{S\ (s/W_1 + 1}$, whereby W_1 is related to the crystal's loaded Q and center frequency. A meaningful derivation of the value of W_1 as a function of the crystal parameters and oscillator sustaining circuit does not exist. Experimental data indicates that an upper bound of W_1 is approximately 0.1 W_o for a crystal VCO with a relatively low loaded Q. The lower bound of W_1 may extend to 800 rad/sec for a high Q crystal that is well decoupled from the oscillator sustaining circuit. The unloaded Q of the tracking loop oscillator crystal will be approximately 3.10^{+6}. The resulting value of W_1 will approach the lower bound. The additional pole will have little significance for loop noise bandwidths of 3, 12, 20 and 48 cps. However, for a loop noise bandwidth of 1000 cps both the crystal VCO pole and the crystal filter poles will alter the ideal loop transfer function (of course the 2KC BPF is easily replaced).

The amplitude and phase response of the tracking loop with 2 B_{LO} = 1000 cps was computed. The loop was optimized at threshold with (limiter suppression) assumed as 0.1. The crystal filter and crystal VCO poles were included. The loop became unstable as $\alpha \rightarrow 1.0$.

4.2 Phase Detector

A high power phase detector was developed in Phase I. The object of this effort was to establish practical dynamic range limits. A single ended phase detector was fabricated at 50 mc as shown in Figure 4.1. The principal design goals of the unit are listed as follows:

1. "The phase detector bandwidth shall be sufficiently wide such that the one sided [illegible] shall be determined only by the IF characteristics". The wideband IF 3DB bandwidth is specified as 6 mc with maximum variations of ± 0.5 within ± 1.5 mc of the center frequency. It follows that the phase detector's 3DB bandwidth must be 3 mc and the response must not vary more than ± 0.5DB from DC to 1.5 mc.

2. The dynamic range shall be sufficient such that the transfer of video output vs signal drive level shall be linear to 50 volts.

The video frequency response achieved is shown in figure 4.2. Further, the linearity and dynamic range of the video output is indicated in figure 4.3.

The video bandwidth is determined by the video output impedance and the bandwidth of the signal driver and its input matching transformer. The bandwidth of the reference drive and associated matching transformer are of little consequence aside from phase stability considerations. The dynamic range is determined by the power capability of the drivers, matching transformers and diodes.

The video output impedance was lowered by replacing the usual video summing resistors with zener diodes. The signal driver bandwidth was achieved by a transmission line transformer and 2C43 vacuum tube driver. The capacitive input of the 2C43 is approximately 7 pf and its linear power capacity 10 watts. The low input capacity minimizes the matching transformer loading and the power capacity contributes to the linear dynamic range of the

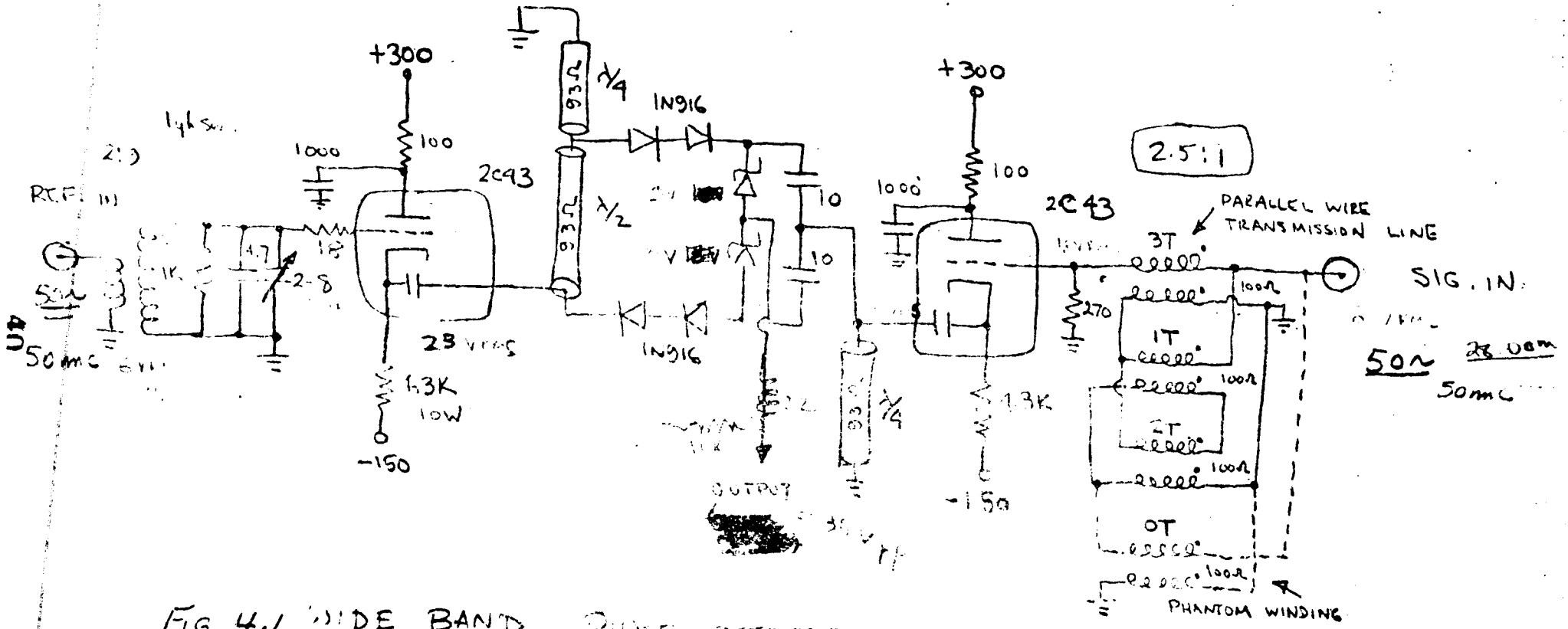


FIG 4.1 WIDE BAND PHASE DETECTOR

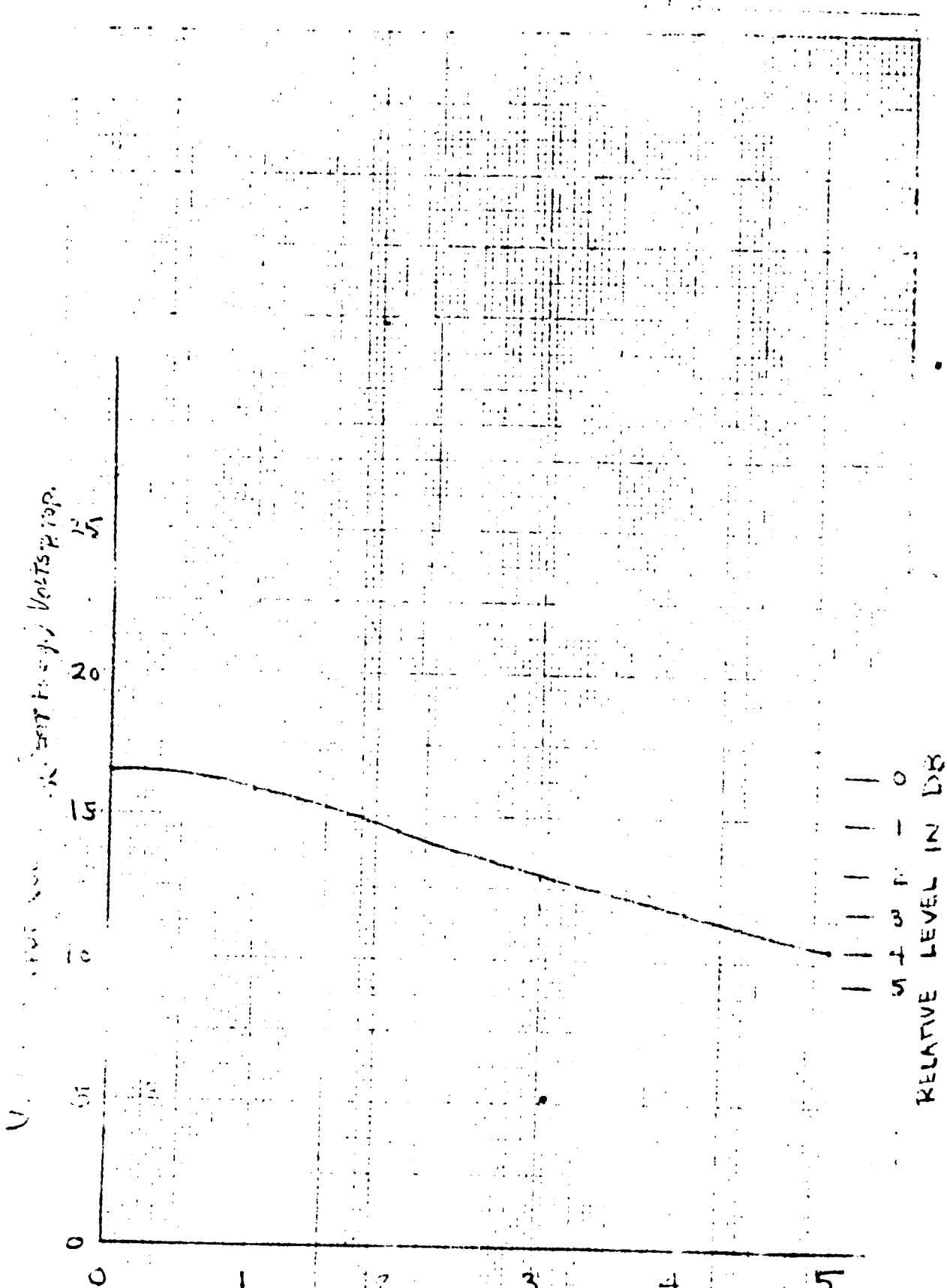
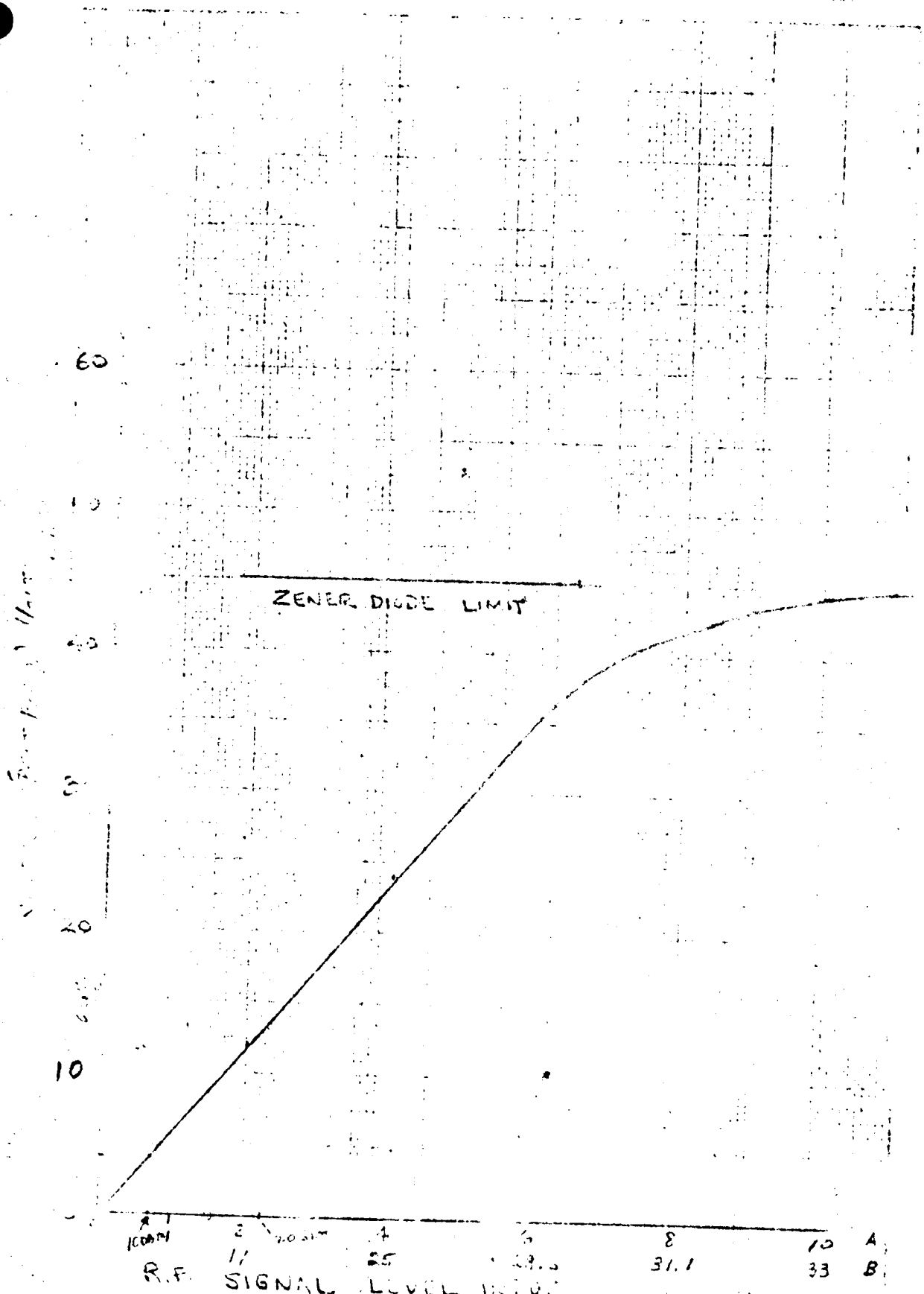


FIGURE 2 - [illegible] DETECTOR VIDEO BANDWIDTH
4.2 CHARACTERISTICS

DATE



R.F. SIGNAL LEVEL IN [illegible]

FIGURE 4.3 LINEARITY OF DIODE DETECTOR VOLTAGE TRANSFER

A) [illegible]
B) [illegible]

CURVE NO.

unit.

As outlined earlier this unit was developed for the wideband demodulator. However, the same techniques are applicable to the tracking loop phase detector and the quadrature phase detector. The bandwidth requirements of these latter units is not stringent; therefore, the drivers will be power transistors. Further, the transmission line transformer will be replaced with a conventional transformer.

4.3 Loop Amplifier

The tracking loop D. C. amplifier contributes the loop amplifier constant, Ka. The loop amplifier constant was assigned the value 32 $\frac{\text{volts}}{\text{volt}}$ for the tracking loop discussed earlier. This particular value of Ka contributed to an open loop gain sufficient to constrain the rms noise static phase error to 1 degree when the transmitter was detuned ± 500 cps from 50 mc. Several loop noise bandwidths are specified. The loop amplifier will be arranged such that the amplifier gain can be varied by substituting different feedback resistors. Other amplifier considerations include drift, bandwidth, overload recovery response and noise. The maximum specified loop noise bandwidth is 1000 cps and the corresponding loop information bandwidth,

150 cps. The D.C. amplifier 3DB bandwidth must be sufficient such that the influence of the amplifier corner is negligible. The amplifier bandwidth must be 150KC to force the amplifier corner 60DB below unity gain when fo is maximum. The amplifier closed loop bandwidth is a function of its closed loop gain. The amplifier must be capable of providing a closed loop voltage gain of 100 and closed loop bandwidth of 150KC simultaneously.

Amplifier drift will result in static phase error between the transmitter standard and VCO. The influence of drift is indicated in figure 4.4.

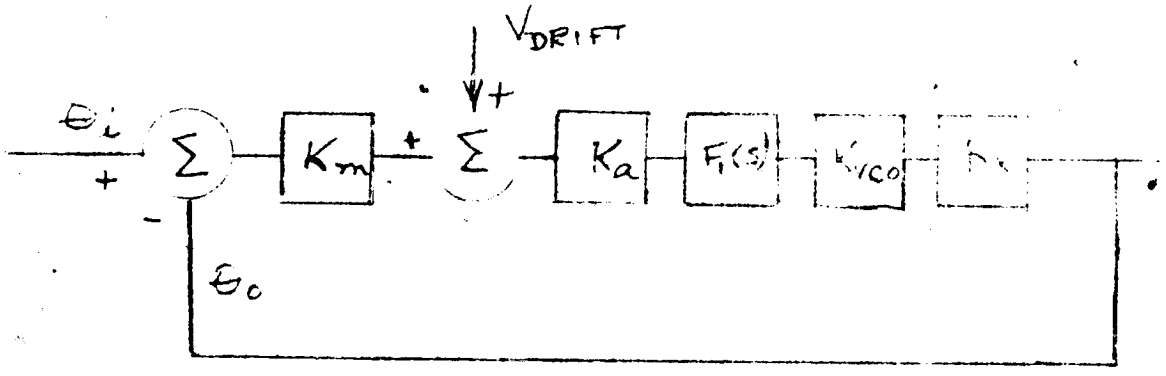


Figure 4.4 Noise Consideration of the Tracking Loop Amplifier

$$\frac{\Theta_o}{V_{DRIFT}} = \frac{K_a F_1(s) K_{VCO} K_x}{1 + K_m K_a F_1(s) K_{VCO} K_x} = \frac{1/K_m}{1 + \frac{1}{K_m K_a F_1(s) K_{VCO} K_x}} \qquad (25)$$

$$IF \quad K_m K_a F_1(s) K_{VCO} K_x >> 1$$

$$\Theta_o = \frac{V_{DRIFT}}{K_m} \qquad (26)$$

A typical value of $V_{(DRIFT)}$ is 100 uv per day for an operational amplifier that is not chopper stablized. The maximum value of Km is 15 $\frac{\text{volts}}{\text{rad}}$. The resulting phase error attributed to drift becomes

$$\Theta_o = \frac{100 \times 10^{-6} \text{ VOLTS}}{15 \frac{\text{VOLTS}}{\text{rad}} \cdot \frac{1 \text{ rad}}{57.3^\circ}} = 0.0382^\circ \quad (\text{no noise}) \qquad (27)$$

If $2B_{LO}$ is 1.0 cps and the noise bandwidth of the crystal filter is 2KC the limiter suppression $\frac{\alpha_o}{\alpha} = \frac{.02}{\alpha}$. The effective loop multiplier constant at threshold becomes $\alpha_o K_m = 0.3 \frac{\text{volts}}{\text{rad}}$. The resulting phase error for the threshold value of Km is 1.9 degrees for 100 uv of loop amplifier drift. This is not acceptable. Stabilized operational amplifiers exhibit a typical 1 uv drift per week compared to the 100 uv per day for the unstabilized units. The resulting phase error contributed by

the loop amplifier drift becomes .000382 degrees and .019 degrees as opposed to .0382 and 1.9 degrees. The loop amplifier shall be chopper stabilized.

The amplifier overload recovery is important during loop pull in. An amplifier voltage gain of 32 was referenced in the loop design. The maximum multiplier constant was 15 $\frac{\text{volts}}{\text{radian}}$. During pull in the amplifier will saturate over a portion of the beat note cycle. Therefore, the time required to respond after over load is important. The loop filter shall precede the amplifier to avoid noise overloading.

The loop amplifier noise contribution is attenuated by the phase detector constant Km in the same manner as the [illegible]. If the phase detector constant is maximum the noise contribution of the phase detector is paramount. However, near threshold the noise contribution of the loop amplifier becomes increasingly important as Km is diminished. Unfortunately, the output noise power density of a transistor is inversely proportional to frequency from D.C. to low audio frequencies (1/f noise). As a result operational amplifiers have a relatively poor noise figure.

Formerly the chopper was a major noise source in stabilized units; however, recent introduction of the photo electric chopper has overcome this fault. A typical rms noise voltage from DC to 1KC is 10 uv. The noise power injected in the loop by the loop amplifier is dependent on the loop noise bandwidth. The amplifier noise contribution in a loop of $2\ B_{LO}$ of 1000 cycles will be approximately 6 uv. At minimum Km (0.3 $\frac{\text{volts}}{\text{rad}}$) the resultant VCO phase jitter becomes

In conclusion, the loop amplifier recovery time must be acceptable and the bandwidth must extend to 150KC at an open loop gain of 100. The closed loop gain must be readily adjustable. The amplifier must be transisterized, chopper stabilized and contribute no more than 10 μv RMS noise (DC to 1KC). Several commercially available amplifiers meet most of those specifications. The Hewlett Packard, Dymec Model DY-2460A is unacceptable because of bandwidth restrictions; however, the unit meets all the other specifications plus convenient variable closed loop gain and an approximate overload recovery

time of 100 usec. The Philbrick P-45 is unacceptable because of drift limitations. The stabilized version of the Philbrick P-45; namely, the SP-456 is advertised as having all the P-45 characteristics plus chopper stabilization. Therefore, this unit shall be the loop amplifier.

4.4 Reference Oscillator

The reference oscillator specification is quoted as follows: "The P.M. receiver reference oscillator shall have a fixed frequency output of exactly 10mc. Its frequency and phase stability shall be consistent with the stability requirements of par. 3.5.1.1.1 and 3.5.1.1.2. The oscillator shall be tunable plus or minus 500 cps".

The referenced paragraphs specify the reference oscillator long term stability as 1 part in 10^{+7} in 1 minute integration interval and 5 parts in 10^{+7} measured over a four hour integration time. The short term stability requirements are specified by par. 3.5.1.1.2 as follows: "The phase stability of the unmodulated transmitter/receiver pair shall be such as to cause no more than three degrees peak error in a noise free phase-coherent receiver with $2P_{LO}$ of 1.0 cps". The long term stability require-

ments refer to each oscillator; namely, the transmitter oscillator and the receiver reference oscillator. The short term stability requirements refer to the combined short term stabilities of the transmitter standard the tracking loop VCO and the reference oscillator.

The long term stability requirements are not particularly difficult to meet. The short term requirements are state of the art. The short term stability of a precision standard is degraded as the crystal is pulled off frequency. The specification indicates that the reference oscillator must be variable ± 500 cycles from 10mc. A precision crystal can be tuned about ± 50 cycles per megacycle. The required tuning range of the reference oscillator is maximum. The specification did not state whether the short term stability spec applies at the center frequency of transmitter/receiver oscillators or at maximum detuning. We assume the former.

The short term stability ($\frac{\Delta f}{f}$) of precision oscillators is specified and measured relative to an averaging time. The averaging time may extend from a few microseconds to several seconds. The averaging time to be considered is related to the tracking loop error e(s) as a function of the noise bandwidth. A plot of 1-H(s) for a tracking loop of $2B_{LO}$ = 1.0 cps indicates the changes in the Reference Oscillator, Transmitter

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Standard and VCO that the loop can correct. The remaining time jitter of any of the three oscillators will contribute to the loop phase error. Figure 4.5 indicates that the tracking loop performs virtually no correction on oscillator jitter that occurs above 1 rad/sec. The loop error decreases at 12 DB/octave from approximately 1 rad./sec to D.C. Therefore, the short term instabilities referenced to averaging intervals of 10 seconds and beyond are important.

There are two principal sources of crystal oscillator phase noise or short term instability; namely, the crystal and the sustaining circuit. The equivalent circuit of a quartz crystal is either a series resonant circuit or parallel resonant circuit depending on the crystal load. For either case, the circuit resistance can be represented by a series resistance which constitutes the crystal's equivalent noise resistance. The short term instability attributed to the resultant noise is expressed by equation 28.

$$\frac{\Delta f}{f} = \frac{2\pi E_N}{\tau f_o E_s} \qquad (28)$$

E_N = Noise voltage

E_s = Signal voltage developed across the crystal terminals

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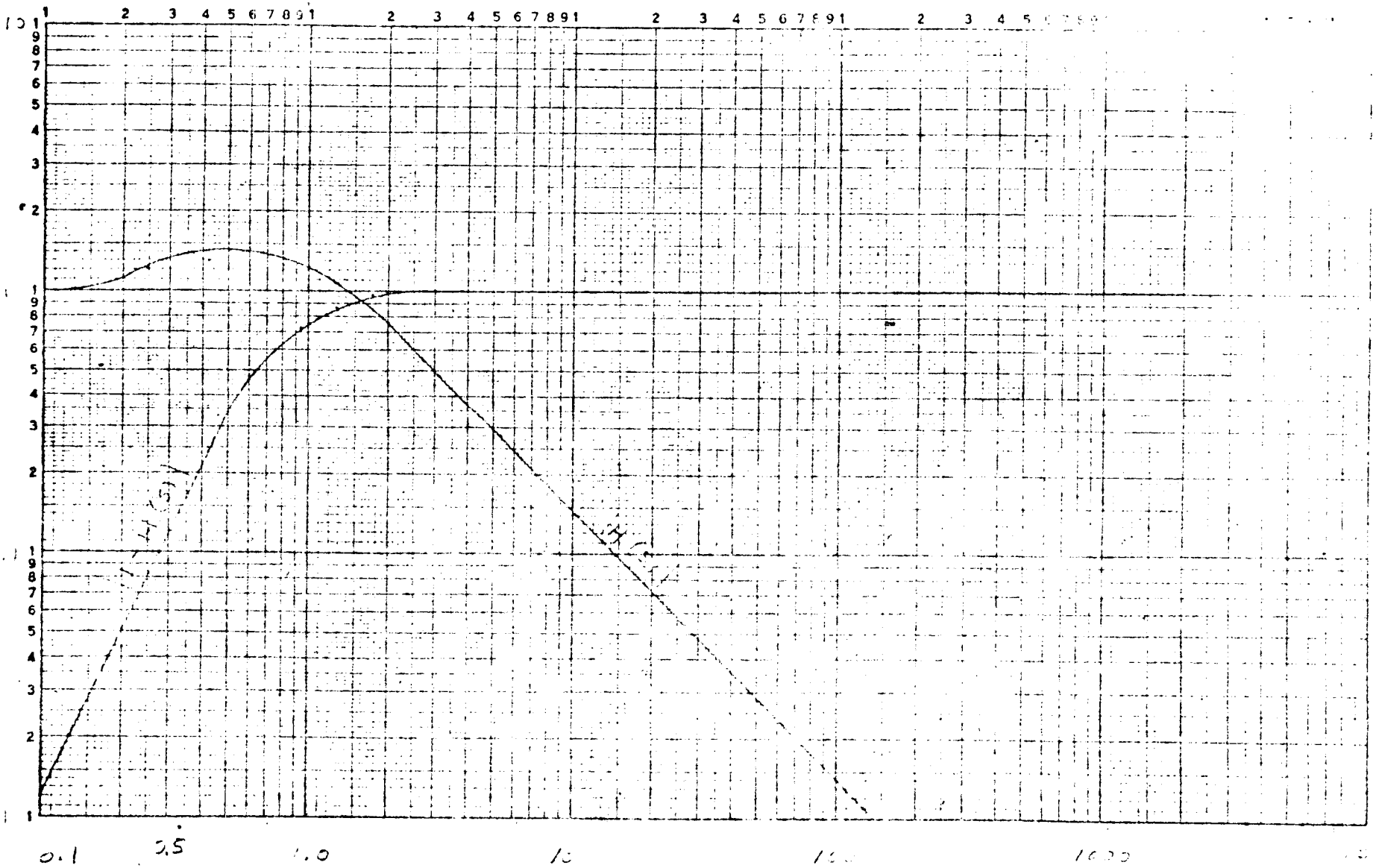
$B_o = 0.943$ $\zeta = 0.704$ $G_o = 3600$ $2B_{Lo} = 1$ cps



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4.5

f_o = Oscillator frequency

τ = Averaging time

$$P_{NOISE} = \frac{E_N^2}{R_{eq}} = 4\,KTB \qquad (29)$$

$$\text{or} \quad E_N = \sqrt{4\,KTB\;Req} \qquad (30)$$

$$E_S = \sqrt{P_{signal} \cdot Req} \qquad (31)$$

$$\frac{\Delta f}{f} = \frac{2\pi}{\tau f_o}\sqrt{\frac{4KTB}{P}} \qquad (32)$$

$$B = \frac{1}{Q} f_o \qquad (33)$$

$$\frac{\Delta f}{f} = \frac{2\pi}{\tau}\sqrt{\frac{4KT}{PQf_o}} \qquad (34)$$

P signal = Signal power dissipated in crystal equivalent series resistance

B = crystal bandwidth

K = Boltzman's constant

T = absolute temperature

Req = crystal equivalent series resistance

Q = crystal storage factor

From equation 34, the short term instability is inversely proportional to the averaging time. Further, a short term stable oscillator must have a large Q and signal drive power. However, higher frequency crystals have a lower Q, therefore the product of f_o Q is more meaningful. Consider a crystal (Bliley BG93A) with the following characteristics:

$Q = (3)\ 10^{+6}$

$f_o = (1)\ 10^{+6}$

$P = (10)\ 10^{-6}$

$T = 350^{\circ}K$ oven temperature

$$\frac{\Delta f}{f} = \frac{2\tau}{\tau} \sqrt{\frac{4 \cdot 1.38 \cdot 10^{-23} \cdot 5}{15^{-5} \cdot 3 \cdot 10^{6} \cdot 10^{6}}} = \frac{1.6 \times 10^{-13}}{\tau}$$

Figure 4.6 indicates a plot of $\Delta f/f$ as a function or the averaging time, τ. This is the theoretical limit of short term stability of the oscillator as established by the crystal.

The sustaining circuit will degrade the theoretical performance of the crystal. The major sources of sustaining circuit noise are listed as

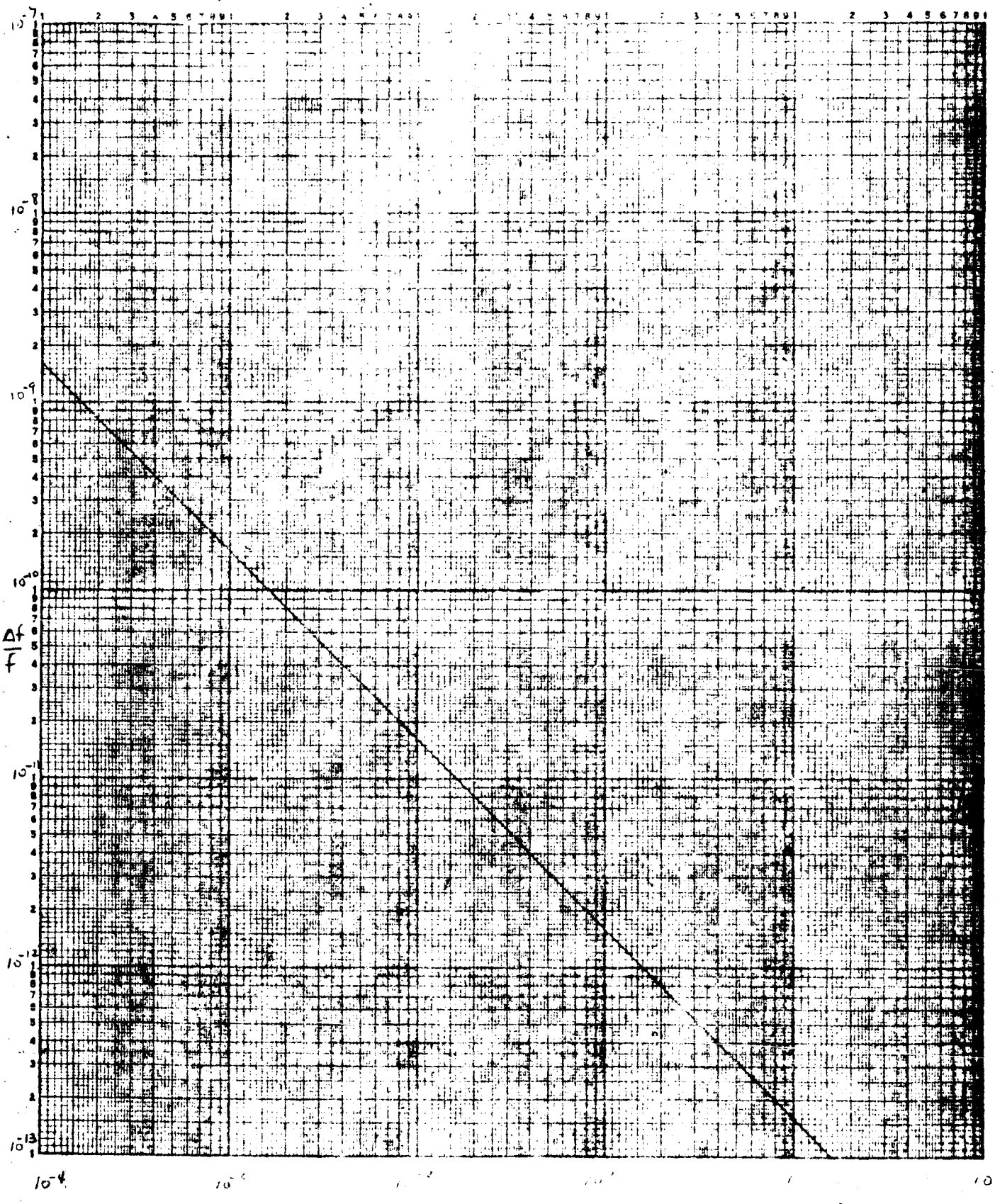


FIGURE 4.6 $\Delta f/f$ vs τ.

follows:

(1) 1/f noise of the transistors (2) power supply ripple (3) stray magnetic fields (4) vibration (5) loading effects (6) temperature regulation of the crystal and associated oscillator circuitry. The latter fault is not usually a problem in dealing with short term stability (long term stability is another matter); however, as outlined earlier an averaging time beyond 10 seconds is meaningful for 2 B_{LO} of 1.0 cps. Therefore, temperature variations over a 10 second period within the proportionally temperature controlled oven are important.

The reference oscillator sustaining circuit under consideration is of the form indicated in figure 4.7.

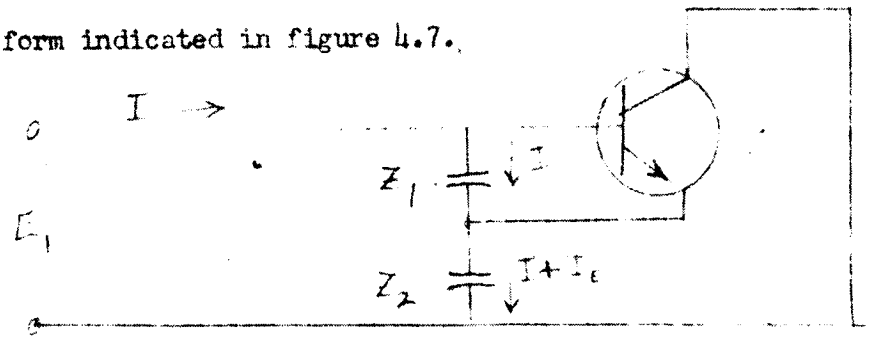


Figure 4.7. Simplified Clapp Oscillator

$$E_1 = I Z_1 + (I + I_E) Z_2 \qquad (40)$$

provided $Z \ll r_i$ transistor input impedance. The transistor emitter-base voltage is $I Z_1$, the base current I / r_b, the emitter current becomes:

$$I_E = \frac{\beta I Z_1}{r_b} \qquad (41)$$

Substituting equation (41) in (40)

$$E_1 = I Z_1 + I Z_2 + \left(\frac{\beta I Z_1}{r_b}\right) Z_2 \qquad (42)$$

The input impedance becomes:

$$Z_{IN} = \frac{E_1}{I} = Z_1 + Z_2 + \frac{\beta}{r_b} Z_1 Z_2 \qquad (43)$$

If Z_1 and Z_2 are capacitors, equation (43) becomes:

$$Z_{IN} = -j X_{C_1} - j X_{C_2} - \frac{\beta}{r_b}\left(-j X_{C_1}\right)\left(-j X_{C_2}\right) \qquad (44)$$

$$Z_{IN} = -j X_{C_1} - j X_{C_2} - \frac{\beta}{r_b} X_{C_1} X_{C_2} \qquad (45)$$

Typical circuit values are: $\beta = 50$, $r_b = 500$, $X_{C_1} = -710$, $X_{C_2} = -j100$. The latter term of equation (45) represents the negative resistance generated by the sustaining circuit. A crystal (in this case

almost series resonant) connected across the input terminals of the sustaining circuit is indicated in the equivalent circuit of figure 4.8.

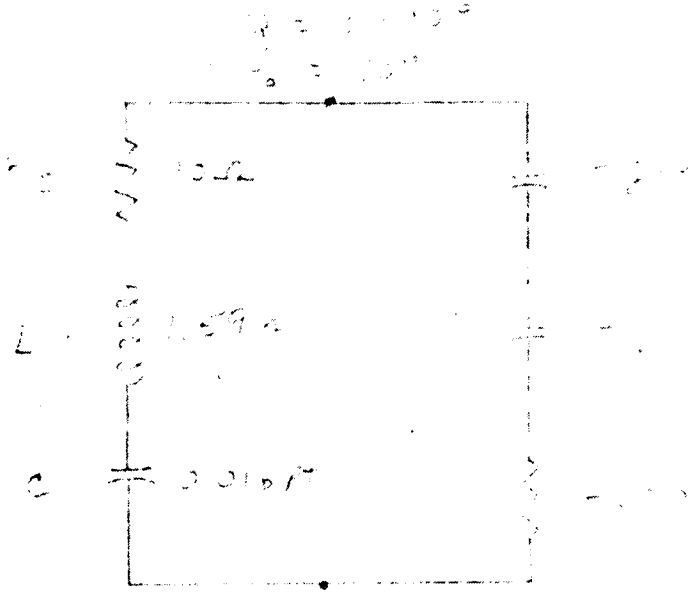


Figure 4.8. Equivalent Circuit of Crystal and Sustaining Circuit

If the negative resistance of the sustaining circuit is greater than the series resistance of the crystal, the circuit is oscillatory at the crystal's resonant frequency modified by X_{c1} and X_{c2}. An inductance whose susceptance cancels the susceptance of X_{c1} and X_{c2} is connected in series with the crystal to cancel the detuning of X_{c1} and X_{c2}.

The sustaining circuit of a precision oscillator is gain controlled such that the forward gain is linear over the complete cycle of the sinusoid.

This is essential as changes in the active devices of the sustaining circuit are never completely decoupled from the crystal (see figure 4.7). Further, the loop gain control accurately establishes the crystal drive power. A simplified diagram of this system is shown in figure 4.9.

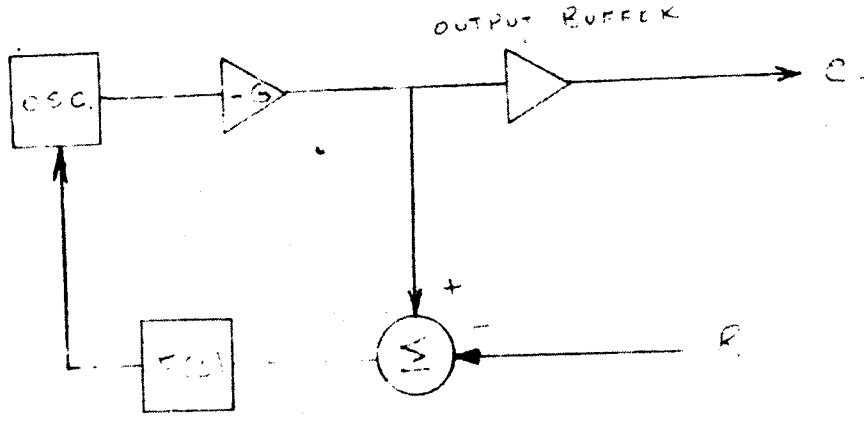


Figure 4.9. Simplified Diagram of Oscillator and AGC System

The system is organized such that a portion of the RF output is rectified, filtered and compared against a reference. The resulting D.C. error controls the crystal drive level by modifying the bias point of the sustaining circuit. Unfortunately, transistor input, output admittances are a function of bias (base current). Further the oscillator stability is slightly modified by changes in the sustaining circuit admittances. The system is improved if the AGC system changes the AC loop gain without changing transistor bias levels. A simplified schematic

of the reference oscillator is indicated in figure 4.10.

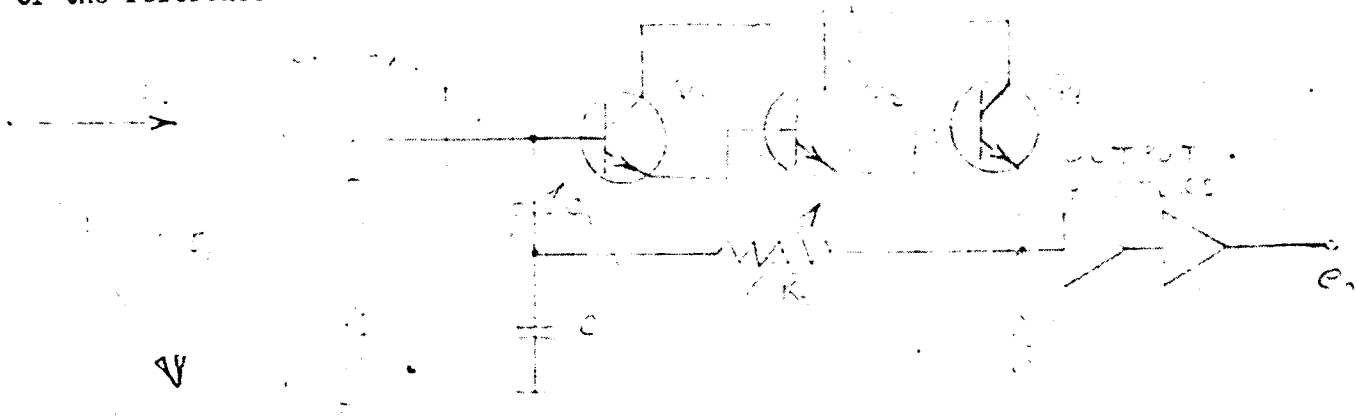


Figure 4.10. Simplified Reference Oscillator

This arrangement is essentially the same as outlined in figure 4.7 and described in equations (50) through (56). The following modifications are noted: (1) three emitter followers provide increased forward gain ($\beta_1\beta_2\beta_3$) and high input impedance (2) The crystal is operated slightly off series resonance and its equivalent circuit is a large inductance in series with a small resistor. A thermistor (R_T) regulates the AC loop gain and crystal drive without modifying transistor bias levels. Low noise high frequency transistors minimize sustaining circuit noise. The emitter followers are inherently gain stabilized and resistant to power supply ripple.

The voltage developed across the crystal (E_S) is relatively large, 2 volts p to p. As shown by equation (28) $\frac{\Delta f}{f}$ is inversely proportional

to E_S. Further, the crystal heating is acceptable as the principal part of E_S is developed across Leq, figure 4.10.

The sustaining circuit provides low output impedance; however, three additional output buffers are provided to further isolate the load from the oscillator. The crystal and sustaining circuit are packaged in a proportionally temperature controlled oven whose temperature is regulated at the crystals turning point. The crystal and sustaining circuit shall be shock mounted and double shielded.

The reference oscillator frequency is specified as 10mc. However, the crystal selected shall be a fundamental, 1mc unit with the characteristics indicated by equations (25) thru (29).

The final 10mc shall be achieved by frequency multiplication of the 1mc oscillator frequency to 10mc. This arrangement is preferred to generating the reference 10mc frequency directly at 10mc with an overtone crystal for the following reason. The specification demands ± 500 cps detuning. An overtone crystal is difficult to pull this percentage frequency and maintain the required short term stability.

The 1mc Transmitter Frequency Standard designed during Phase I included the previously mentioned considerations. The same techniques will be applied to the Receiver Reference Oscillator and VCO.

A detailed schematic of the 1mc reference oscillator is indicated in figure 4.11. A comparison of the measured short term stability and theoretical limit is indicated by figure 4.12.

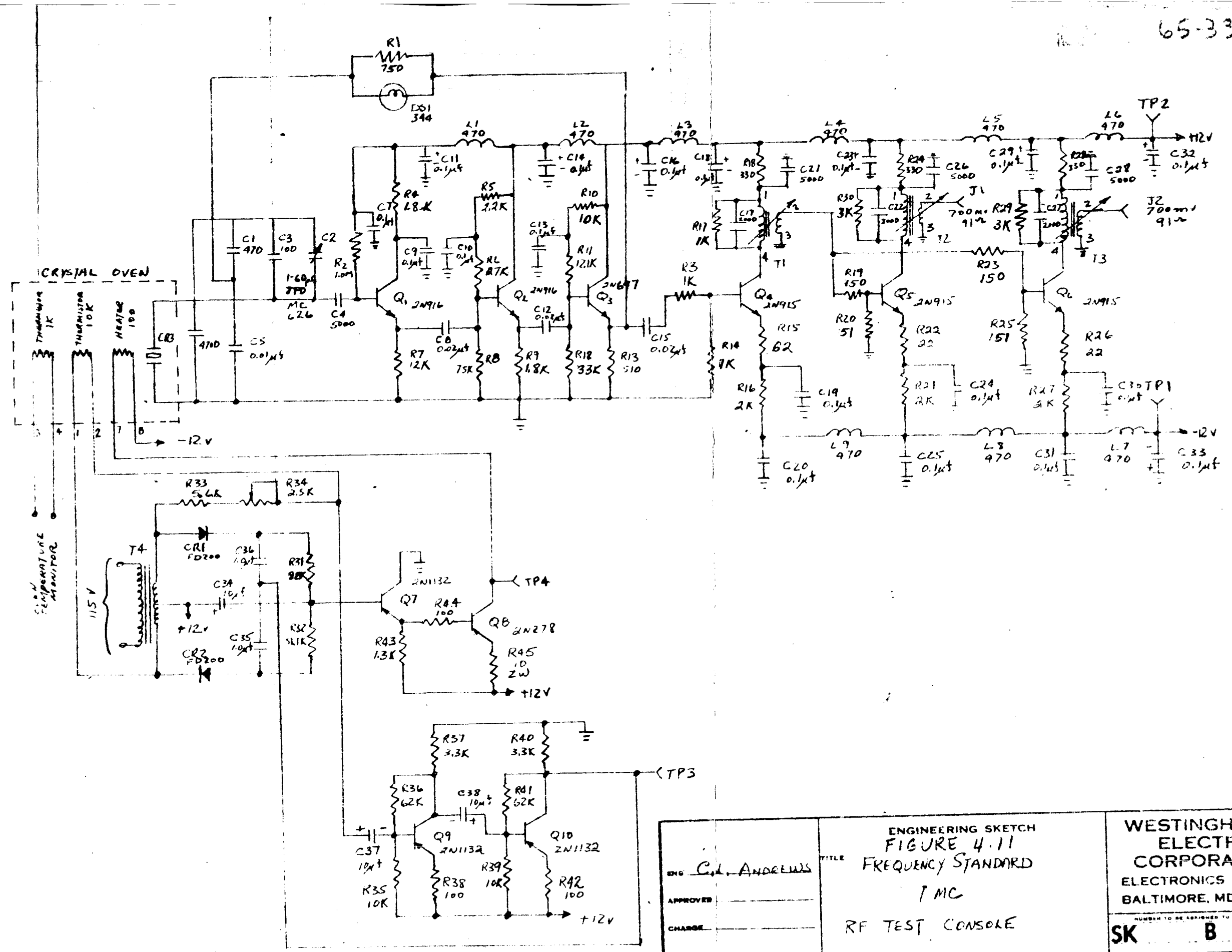
The short term stability of the oscillator for averaging times less than 1.0 sec. is acceptable. The divergence of experimental and theoretical data at longer averaging times is unacceptable. The data indicates that the sustaining circuit meets the various requirements outlined earlier. However, the short term instability contributed by the oven circuitry and oven packaging is unacceptable. Corrective measures include: 1. an improved oven servo reference (internal 1KC oscillator instead of 60 cycle line voltage) 2. Improved packaging whereby both the crystal and sustaining circuit are mounted in the oven.

The details of the measurement test procedure used to measure the experimental data indicated in figure 4.12 is included in the Test Plan and Test Instrumentation Report, Appendix K.

The previous discussion outlined the necessary characteristics of a short term stable oscillator. The various means of achieving these characteristics were listed. However, the most difficult portion of the short term stability specification does not mention short term stability directly but rather specifies allowable phase noise in the tracking loop.

The long term stability specification is not particularly stringent (5 parts in 10^{+7} per four hour period.) The long term stability of the oscillator discussed was compared to a standard that in turn is calibrated to the ground wave of WWV. The long term stability test set is outlined in figure 4.13. The long term stability of the test oscillator was recorded as 3 parts in 10^{+8} over a 19 hour period.

The following exceptions are taken to JPL spec. GPG-15062-DSW par. 3.5.1.12: "The phase stability of the unmodulated transmitter/receiver pair shall be such as to cause no more than a three (3) degree peak phase error



ENG C.L. ANDREWS APPROVED CHARGE	ENGINEERING SKETCH TITLE FIGURE 4.11 FREQUENCY STANDARD 1 MC RF TEST CONSOLE	WESTINGHOUSE ELECTRIC CORPORATION ELECTRONICS DIVISION BALTIMORE, MD. U. S. A. NUMBER TO BE ASSIGNED TO FINAL DRAWING SK B SHEET OF SHEETS

FIGURE 16 FREQUENCY STANDARD SCHEMATIC

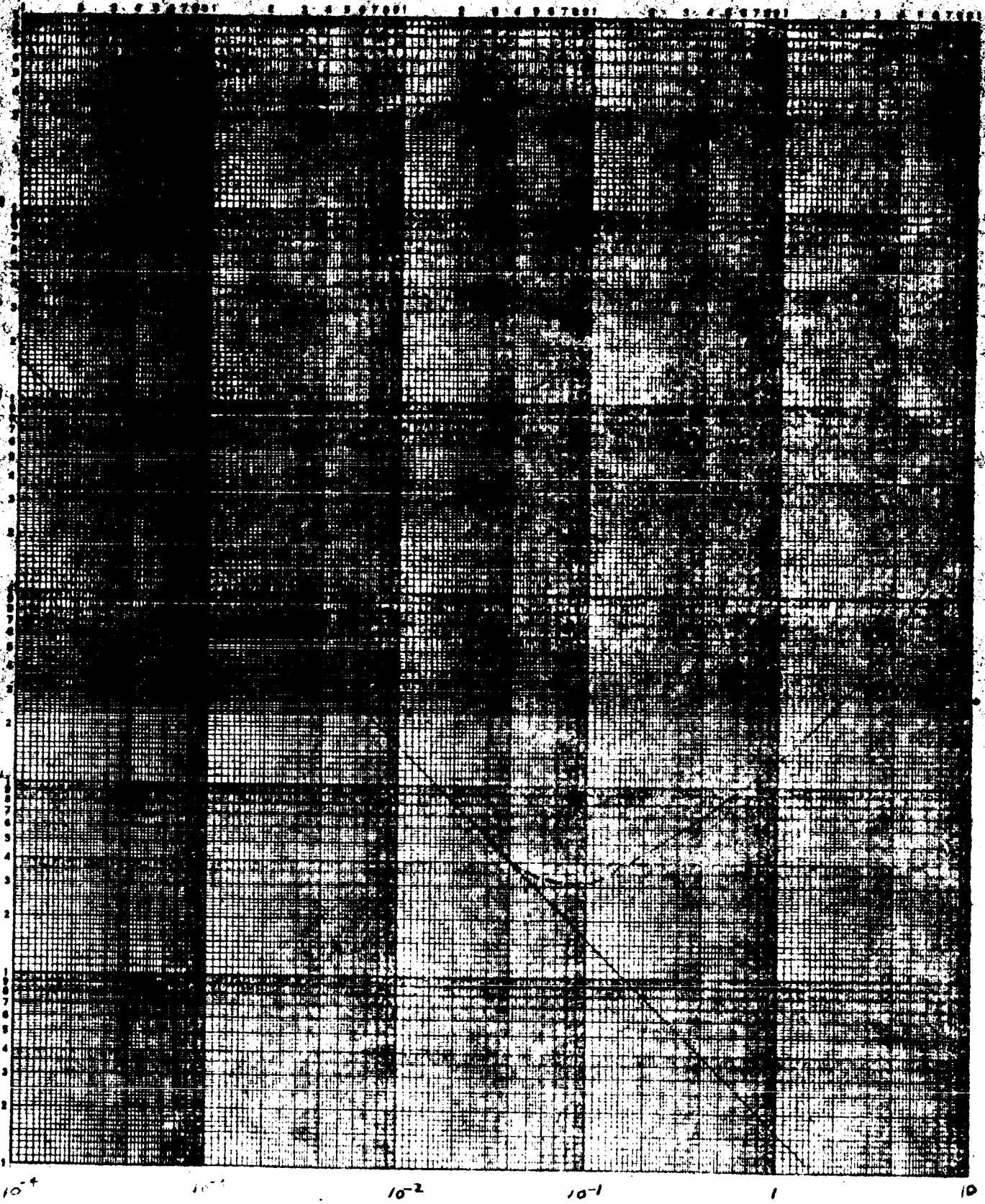
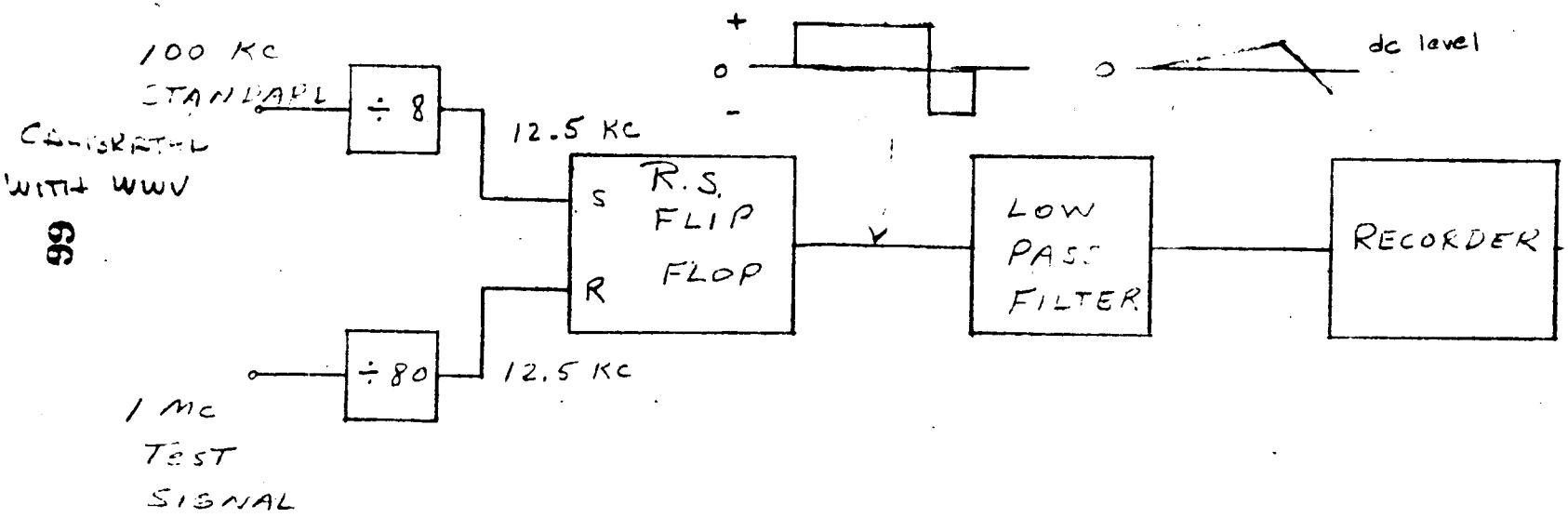


FIGURE 4.12 COMPARISON OF MEASURED SHORT TERM STABILITY AND THEORETICAL LIMIT



99

FIGURE 4.12 LONG TERM STABILITY TEST SET

(1 MC TEST SIGNAL CHANNEL)

in a noise-free phase coherent receiver with a 2 BL of 1.0 cps". Westinghouse requests that the specification be changed to the following:

"The phase stability of the unmodulated transmitter/receiver pair shall be such as to cause no more than a one (1) degree RMS phase error in a noise-free phase coherent receiver with 2 B_{LO} of 3.0 cps." The specification change is requested for the following reasons (1) RMS noise voltage is a more meaningful measurement (2) As outlined earlier, the short term stability is referenced to an averaging time that is inversely proportional to the tracking loop noise bandwidth. The oven regulation is the principal contributor to instabilities at the longer averaging time. We are not confident that the oven regulation can be built to meet the requirements of 2 BL = 1.0 cps. Measurements indicate that the improvements discussed earlier will enable the reference oscillator to meet the instabilities dictated by a loop noise bandwidth of 3.0 cps.

4.5 Frequency Multipliers

The reference oscillator shall be Inc for the reasons outlined in section 3.1.4. Two steps of frequency multiplication x5 and x7 shall be

used to achieve the 10mc reference frequency. The power gain of each multiplier is approximately unity. The parameters of interest include short term stability and harmonic rejection.

A simplified block diagram of the basic frequency multiplier is shown in figure 4.14.

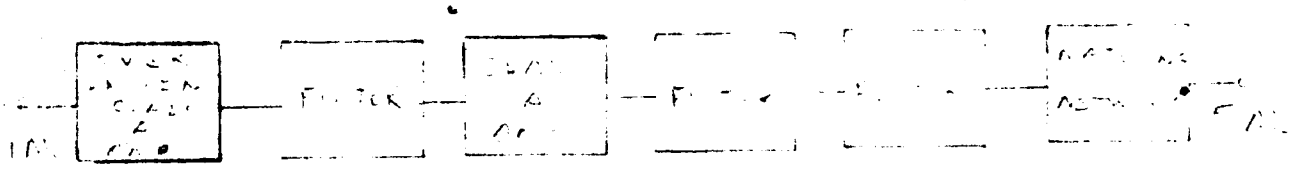


Figure 4.14. Frequency Multiplier

The short term instability (phase noise) of the frequency multipliers contributes to the short term instability of the 10mc reference source. The multiplier characteristics included in the design that contribute to excellent short term stability include; (1) overdriven class A amplifier harmonic generator (2) class A voltage amplifier and buffer (3) magnetically shielded cup core transformers. The latter precaution provides protection

against stray magnetic fields that may thread the windings of an open transformer and induce incidental angle modulation.

The harmonic suppression referenced to the output frequency is achieved by interstage and output filtering. The first two interstage filters are transitionally coupled two pole networks designed to reject the closest harmonic 40DB. Each transistor is coupled to its interstage such that the transistor input output susceptance is absorbed as a portion of the filter reactance. The transistor input output conductance is transformed 1.4, transistor to filter, to minimize filter loading. The resultant harmonic rejection with respect to the output of the 1-5mc multiplier is indicated in figure 4.15.

Frequency (mc)	Referred to 5mc
1 mc	-90 DB
2	-80
3	-81
4	-90
5	0
6	-90

7	-90
8	-90
9	-90
10	-65
15	-90
20	-90
25	-90

Figure 4.15. Spurious Levels 1-5mc Frequency Multiplier

A detailed schematic of the 1-5mc multiplier is shown in figure 4.16. The multiplier is shielded and packaged as a replaceable module. The unit was developed during Phase I.

The phase noise contributed by two multiplier chains (fabricated as described) yielded 0.70RMS degrees of phase noise in a simulated 2 B_{LO} of 3.0 cps. The test set for this measurement is indicated in figure 4.17.

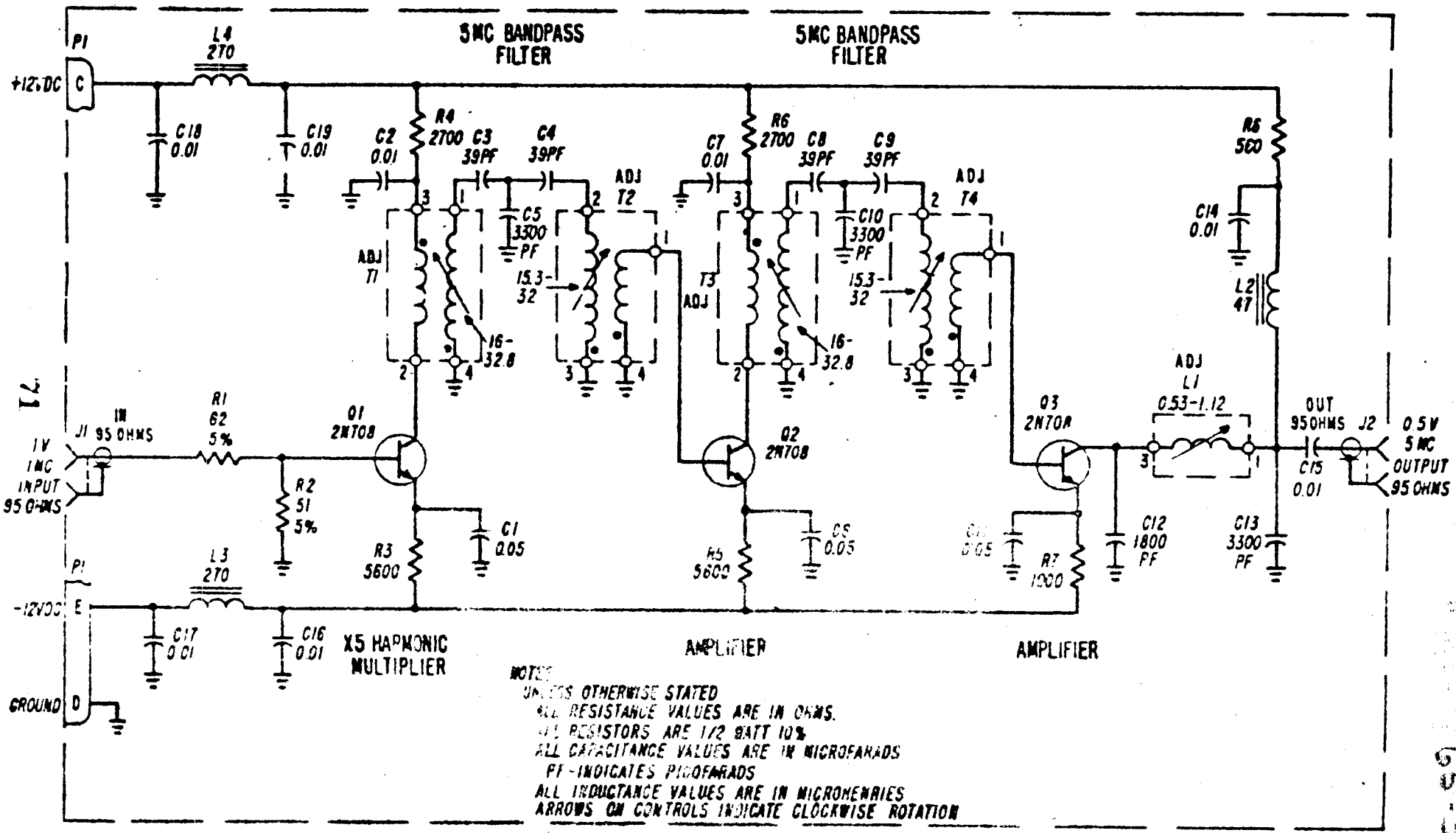


Figure 17. Schematic 1 to 5 MC Multiplier

4 16

follow ± 500 cps transmitter detuning. However, par. 3.5.1.3.7 states that the loop gain must remain within ± 3% over the same transmitter detuning range. Clearly the characteristic of figure 4.18 is not linear to within ± 3%. There are two alternatives. First, a diode function generator between the loop amplifier and VCO will approximate, by straight line segments, an overall linear transfer of VCO frequency to control voltage. The final accuracy of the transfer is dependent on the number of segments. This system is a common technique used on analog computers to synthesize log, square root, square, etc. functions. This system will yield a typical full scale (± 10 volts) accuracy of ± 1%. This system is expensive and complicated as the diode function generator is usually arranged to shape the input impedance of an operational amplifier as a function of the input voltage.

An alternate approach is available as a result of recent voltage variable capacitance development. The HPA division of Hewlett Packard has developed the [illegible] diode which exhibits a linear transfer of capacitance vs control voltage over a restricted dynamic range. It follows that the L/C ratio of a crystal oscillator is so large that a linear change in C as a

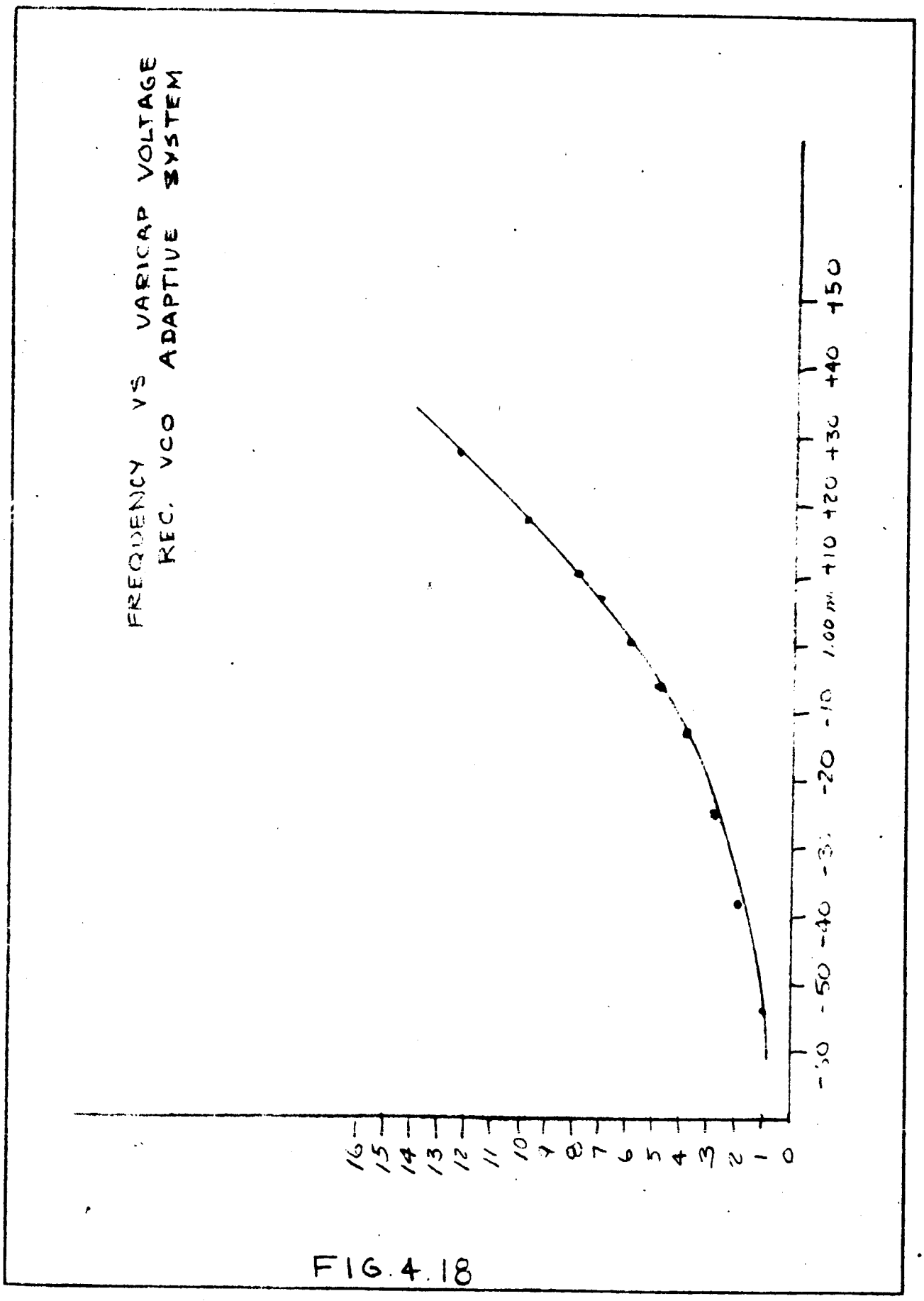

FREQUENCY VS VARICAP VOLTAGE
REC. VCO ADAPTIVE SYSTEM
-50 -40 -30 -20 -10 1.00 +10 +20 +30 +40 +50
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

FIG. 4.18

ADDITIVE VCO

VARICAP VOLTAGE	FREQUENCY
1.0	999,946.2
2.0	999,961.9
3.0	999,974.0
4.0	999,983.8
5.0	999,992.2
6.0	999,999.4
7.0	1,000,005.3
8.0	1,000,011.0
10.0	1,000,020.6
12.0	1,000,028.6
15.0	1,000,039.6
30.0	1,000,071.6

FIG. 4.19

function of control voltage will yield an approximately linear change in frequency. The latter approach is obviously more desirable; however, to date no data exists to support enthusiasm.

4.7 First IF Amp and Crystal Filter

The gain and small signal linear power capability of the tracking loop first IF amplifier are listed by the figure 2.3 level diagram as +31DB and 0BEM, respectively. The specified 3DB bandwidth is 2KC. The phase response must be symmetrical within $\pm 3^{\circ}$ for frequencies $\pm$ 6KC of center frequency. Further, the bandwidth must be changeable by plug-in module. A later addition to the spec. indicates the following: "The wideband and narrowband IF amplifiers must track in phase $\pm 2^{\circ}$ over all operating conditions including noise biasing".

The basic IF amplifier building block will be a broadband feedback pair or doublet. This unit utilizes both source/load impedance control and feedback to achieve stable power gain. Figure 4.20 indicates the basic stage configuration

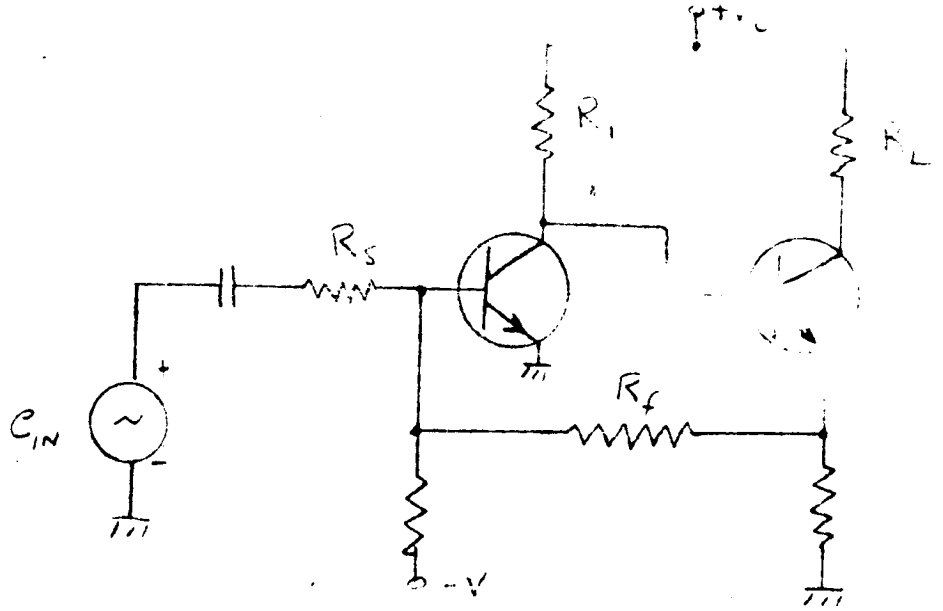


Figure 4.20. Feedback Pair

The principal parameters of interest include:

1. 3DB Bandwidth, 1KC—80Mc 2. Gain Stability, 1 DB over a temperature range of -55°C to +100°C 3. Power gain per stage 10 to 25DB per stage depending on feedback 4. Linear Small Signal power capability ODBM 5. Noise Figure 8DB

The first IF amplitude and phase response specified will be established by a crystal filter using two cascaded two crystal semi-lattices. The narrow bandwidth will yield arithmetic symmetry well past the ± 6KC points. The insertion loss will be 2-4DB.

The combination of three cascaded feedback pairs and crystal filter,

in our opinion, will yield an IF amplifier that is both gain and phase stable and resistant to incidental angle modulation as a function of power supply ripple. However, the phase characteristic of the narrow band IF and the wideband IF are established by their respective input filters. The 3DB bandwidths are 2KC and 6MC. The relative phase responses will not meet the specified phase tracking specification either in the presence of noise or otherwise, however, the resultant phase error can be nulled with the reference frequency phase shifter.

4.8 Limiter

The gain, dynamic range, limit level and linear power capability of the tracking loop limiter is listed in the figure 2.3 level diagram as 42DB, 36DB ODBM and ODBM respectively.

Two basic tunnel diode limiters have been developed by Westinghouse that are applicable. The simplified schematics and corresponding characteristics are shown in figures 4.21 and 4.22.

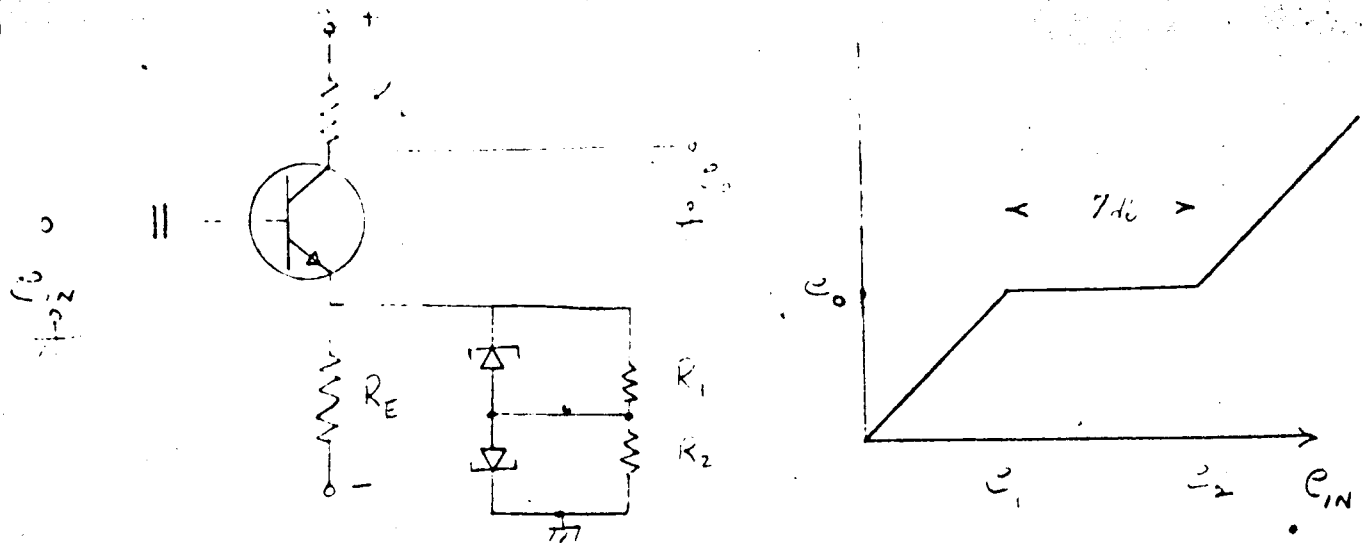


Figure 4.21 Tunnel Diode Limiter CKT 1

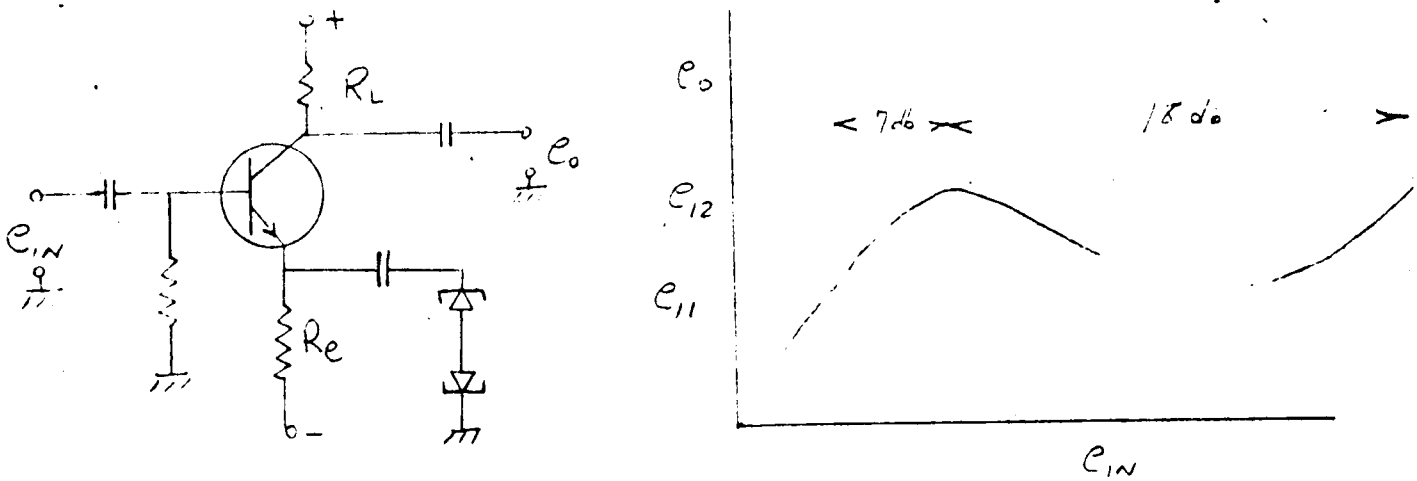


Figure 4.22. Tunnel Diode Limiter CKT 2

If the limiter figure 4.21 is preceded by the limiter figure 4.22 the overall characteristics of figure 4.23 results.

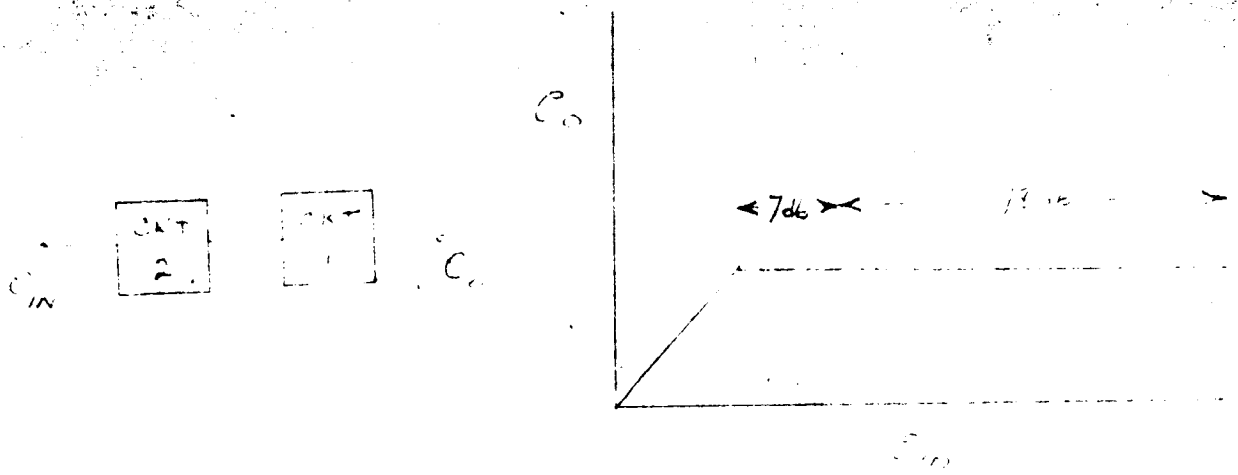


Figure 4.23 Cascaded Tunnel Diode Limiter

Cascading additional stages of CKT2 simply adds 18DB of dynamic range and 7DB of gain per stage. Therefore, a limiter chain consisting of five stages of CKT2 terminated by one stage of CKT1 will yield 42DB of gain and 96DB of dynamic range. An eight stage tunnel diode wideband limiter was built using this technique. The characteristics are listed as follows:

1.	Gain	60DB
2.	Input Dynamic Range	60DB
3.	Limit Level	200 mv (± 0.25% variation over 60DB input range)
4.	Frequency Tested	Up to 100MC
5.	Bandwidth	30MC
6.	Power Dissipation	1/4 watt

A comparable limiter patterned after the work of Ruthroff[1] was fabricated.

A typical amplifier limiter stage is shown in figure 4.24. Four stages were cascaded and the following characteristics achieved.

1.	Gain	60DB
2.	Input Dynamic Range	60DB min
3.	Limit Level	200 [illegible] (negligible variation with 60DB input change)
4.	Frequency Tested	up to 100MC
5.	Bandwidth	20MC
6.	Power Dissipation	3 watts

The comparative phase shift of both limiters was measured at 30MC over 50DB change of input. The tunnel diode limiter exhibited 17 degrees of phase shift while the conventional limiter phase shifted the 30MC signal 35 degrees over the same dynamic range of input. A comparable test for shift in limit level as a function of temperature variation was conducted.

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(1) "Amplitude Modulation Suppression in FM Systems" by C. I. Ruthroff, The Bell System Technical Journal, July 1950.

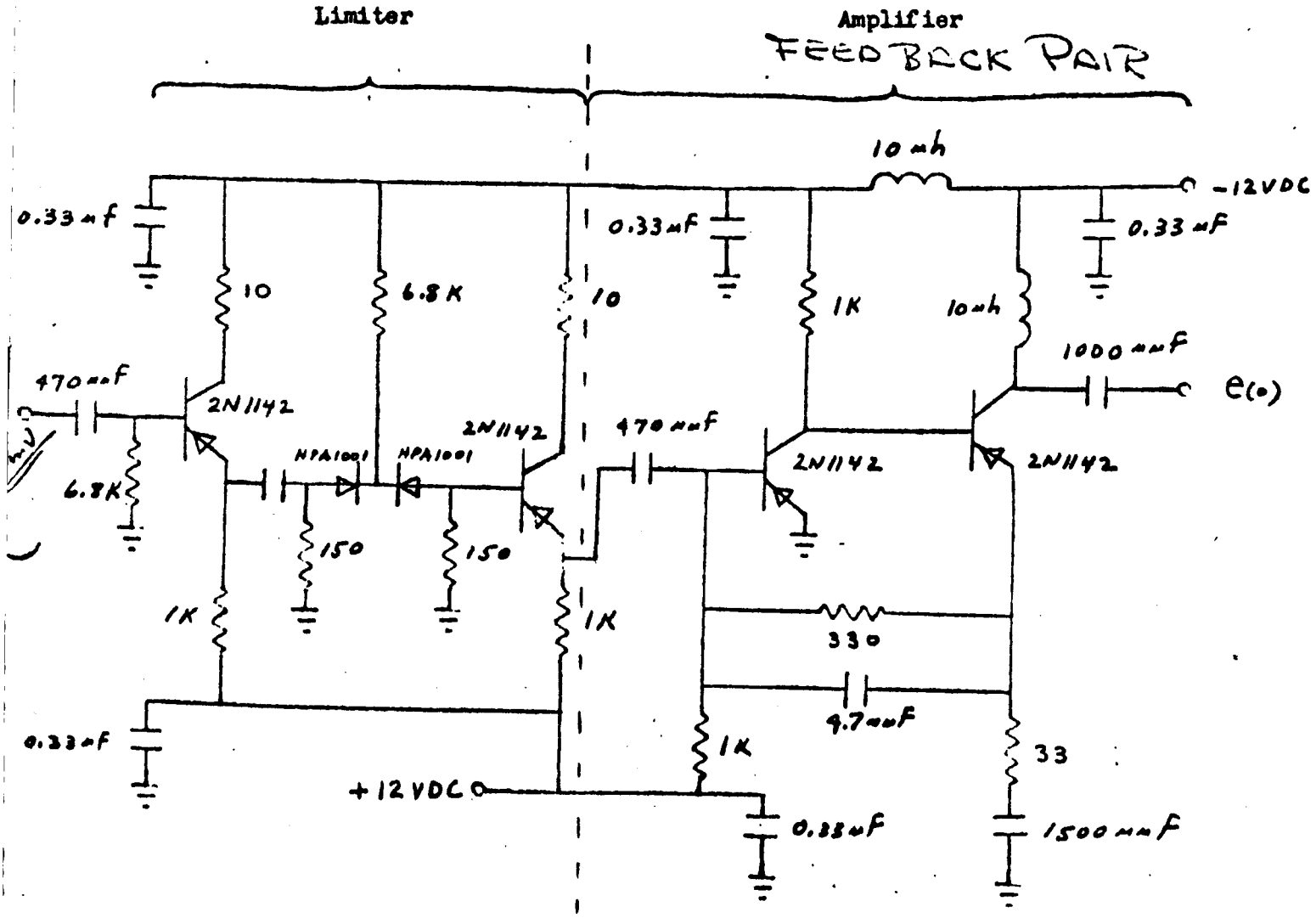

FIGURE 4 (Basic conventional limiter-amplifier circuit)

The tunnel diode limiter limit level shifted 5.4% from 200 mv over a temperature range of -30°C to +70°C. The conventional limiter limit level shifted 20% from 200 mv over the same temperature level. The tunnel diode limiter is less temperature sensitive and yields less phase shift as a function of drive level; however, the limit level variation as a function of drive level is inferior to the conventional limiter.

The tunnel diode limiter approach will be applied to the RF Test Console.

4.6.1 Second IF Amplifier

The required gain and linear power capability of the Second IF Amplifier are listed on rows 1 and 10 of figure 2.3 as 20DBM and 23DBM, respectively. The required power capability is beyond the capacity of the medium power "Feedback Pair". The power amplifier developed by Westinghouse shown in figure 4.25 exhibits most of the required characteristics. This unit is not directly applicable but at least provides a basis for refinement. The amplifier parameter of interest includes:

1) Gain	11DB
2) Large Signal Linearity	3DB compression of 0.25VRMS Input at f_1 when 10VRMS input

R.F. AMPLIFIER SCHEMATIC

KMS-101

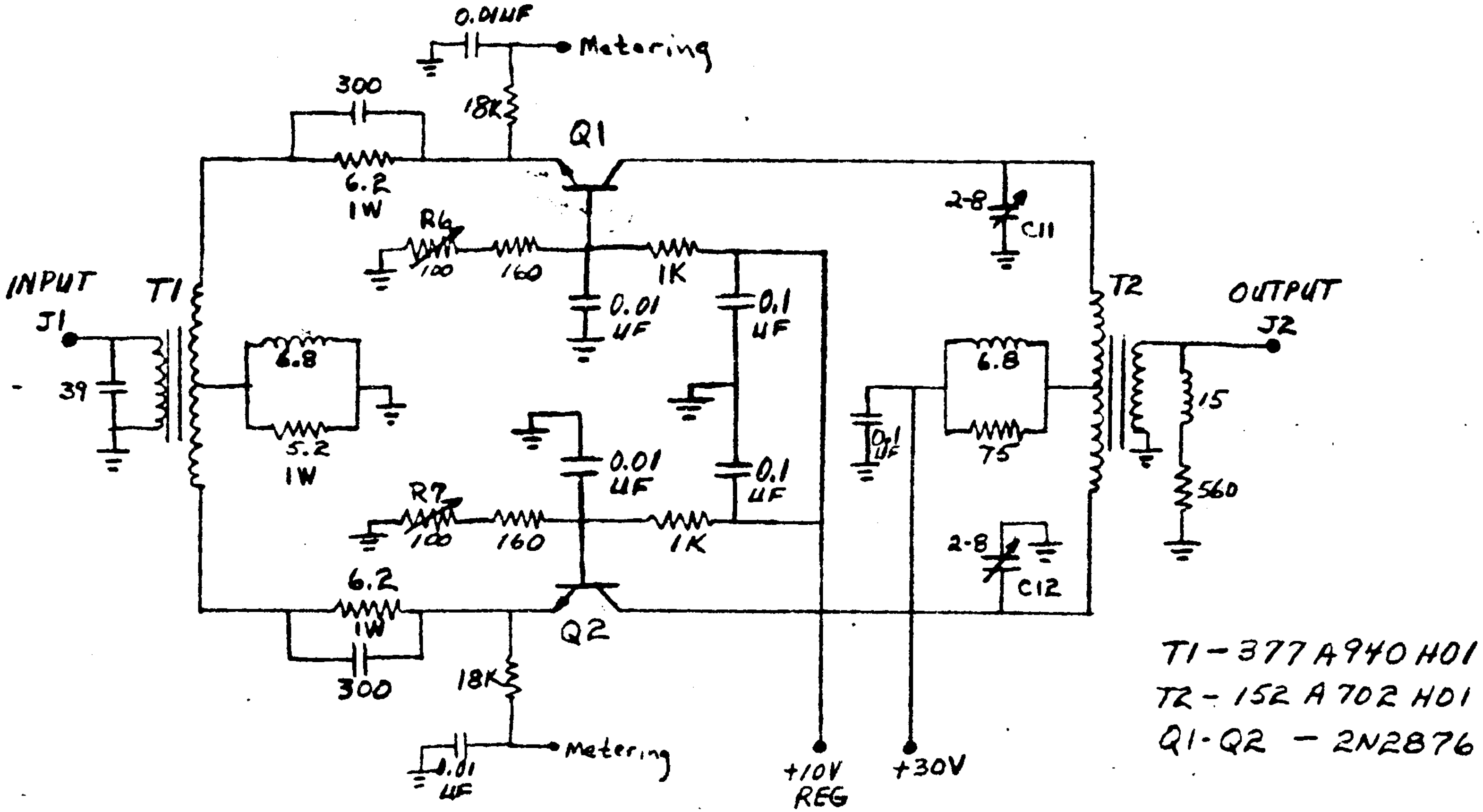

Figure 4.25

H.A. MALE
12/19/63

	at f_2 applied. f_1 and f_2 constrained to the band 2-32MC
3) 3DB Bandwidth	2-32 MC
4) Small Signal Output Power Capability	2 watts
5) Compression at 2 watt output	Unknown
6) Phase Response and Phase Linearity	Unknown
7) Intermodulation products of two 0.25 VRMS inputs	70DB
8) Noise Figure	8DB

The phase and amplitude response and stability, at least over the band 10 MC ± 100 KC plus the compression at the 2 watt output level must be more thoroughly investigated. This data is essential before a meaningful decision regarding the application of this amplifier to the tracking loop second IF can be made.

4.9 Mixer

The mixer specification is repeated as follows: "The PM Receiver balanced modulators shall be functionally equivalent to ideal voltage multipliers in the time domain or translators in the frequency domain such

that all spurious and feedthru products are 60 DB below the desired output".

The mixer can be analyzed as a non-linear device whose non-linearity characteristic is represented by either a power series or a piecewise linear characteristic.

Consider the power series representation. The non-linear characteristic is represented by retaining four terms of a power series.

$$e_o = a_1 e_1 + a_2 e_1^2 + a_3 e_1^3 + a_4 e_1^4 + \cdots \qquad (46)$$

The mixer inputs are considered as follows:

$$C + S + T = C_o \cos c + S_o \cos s + T_o \cos t \qquad (47)$$

The angles c, s and t are considered a measure of frequency with time omitted for convenience. C represents the mixer local oscillator while S and T represent two frequencies within the information spectrum. When this input function is substituted into four terms of the power series the following results.

$$V = a_o + a_1 (C + S + T) + a_2 (C + S + T)^2 + a_3 (C + S + T)^3 + \cdots \qquad (48)$$

The terms of the power series have been expanded and the resulting frequencies and coefficients tabulated in table 4.1. The table indicates that the coefficients of the sideband pair c + s and c - s are:

(49)

For a mixer followed by a filter tuned to either (c + s) and (c + t) or (c - s) and (c - t) where s and t are sideband tones very close together, nearly all the distortion products will be rejected by the filter. However, there are some combinations of c $\pm$ 2 s $\pm$ t and c $\pm$ 2t $\pm$ s which fall within the filter passband and appear as distortion of the desired signal. The coefficients of these frequency components are:

$$\frac{3 a_4 C_0 S_0^2 T_0}{2} \qquad (50)$$

and

$$\frac{3 a_4 C_0 T_0^2 S_0}{2} \qquad (51)$$

The latter terms constitute the spurious and feedthrough referenced in the specification. The principal point indicated by this exercise is that the magnitude of the spurious components that fall within the passband are a

function of the square of the magnitude of the original mixer input spectrum. The magnitude of the desired mixer sideband output (c + s), (c - s) or (c + t), (c - s) is a function of the magnitude of the mixer input spectrum raised to the first power. Therefore, if the mixer input spectrum level is diminished, the desired output sideband level decreases as a direct function of the input level, where as the inband distortion decreases as the square of the input level. Therefore, the following conclusions are evident. If a mixer can be built with a non-linear characteristic that is accurately described by the first two terms of a power series, the resulting spectrum will contain no inband distortion terms. Further, if additional power series terms are present the inband distortion terms are reduced more rapidly than the desired sidebands by simply reducing the mixer signal drive. The PM receiver mixer drive level is listed as -64 DBM in column 10 of figure 2.3.

The piecewise linear mixer is considered in the following discussion. A typical balanced mixer (suggested by the specification) is shown in figure 4.26.

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FREQUENCY	COEFFICIENT			
$c+s$ $c-s$	$a_2 C_0 S_0$	$\frac{3a_4 C_0^3 S_0}{2}$	$\frac{3a_4 C_0 S_0^3}{2}$	$3a_4 C_0 T_0^2 S_0$
$c+t$ $c-t$	$a_2 C_0 T_0$	$\frac{3a_4 C_0^3 T_0}{2}$	$\frac{3a_4 C_0 T_0^3}{2}$	$3a_4 C_0 S_0^2 T_0$
$s+t$ $s-t$	$a_2 S_0 T_0$	$\frac{3a_4 S_0^3 T_0}{2}$	$\frac{3a_4 S_0 T_0^3}{2}$	$3a_4 S_0 C_0^2 T_0$
$c-s-t$ $c-s+t$ $c+s-t$ $c+s+t$	$\frac{3a_3 C_0 S_0 T_0}{2}$			
$2c-s$ $2c+s$	$\frac{3a_3 C_0^2 S_0}{4}$			
$2c-t$ $2c+t$	$\frac{3a_3 C_0^2 T_0}{4}$			
$2s-c$ $2s+c$	$\frac{3a_3 S_0^2 C_0}{4}$			
$2t-c$ $2t+c$	$\frac{3a_3 T_0^2 C_0}{4}$			
$2t-s$ $2t+s$	$\frac{3a_3 T_0^2 S_0}{4}$			
✓ $2c+2s$ $2c-2s$	$\frac{3a_4 C_0^2 S_0^2}{4}$			
$2s+2t$ $2s-2t$	$\frac{3a_4 S_0^2 T_0^2}{4}$			
$2t+2c$ $2c-2t$	$\frac{3a_4 T_0^2 C_0^2}{4}$			

TABLE 41

FREQUENCY	COEFFICIENT			
$2C-2A+t$ $2C+2A+t$	$\frac{3a_4 C_0^2 S_0 T_0}{2}$			
$2C-2A+t$ $2C+2A-t$				
$2B-C-A$ $2A+C+t$ $2A+C-t$ $2A-C+t$	$\frac{3a_4 S_0^2 C_0 T_0}{2}$			
$2t-C-A$ $2t+C+A$ $2t-C+A$ $2t+C-A$	$\frac{3a_4 T_0^2 C_0 S_0}{2}$			
$3C+A$ $3C-A$	$\frac{a_4 C_0^3 S_0}{2}$			
$3C+t$ $3C-t$	$\frac{a_4 C_0^3 T_0}{2}$			
$3A+C$ $3A-C$	$\frac{a_4 S_0^3 C_0}{2}$			
$3A+t$ $3A-t$	$\frac{a_4 S_0^3 T_0}{2}$			
$3t+C$ $3t-C$	$\frac{a_4 T_0^3 C_0}{2}$			
$3t+A$ $3t-A$	$\frac{a_4 T_0^3 S_0}{2}$			

TABLE II (CONT'D)

FREQENCY	COEFICIENT			
r.	$a_1 C_0$	$\frac{3a_3 C_0^3}{4}$	$\frac{3a_3 C_0 S_0^2}{2}$	$\frac{3a_3 C_0 T_0^2}{2}$
p.	$a_1 S_0$	$\frac{3a_3 S_0^3}{4}$	$\frac{3a_3 S_0 C_0^2}{2}$	$\frac{3a_3 S_0 T_0^2}{2}$
t	$a_1 T_0$	$\frac{3a_3 T_0^3}{4}$	$\frac{3a_3 T_0 S_0^2}{2}$	$\frac{3a_3 T_0 C_0^2}{2}$
2r.	$\frac{a_2 C_0^2}{2}$	$\frac{a_4 C_0^4}{2}$	$\frac{3a_4 C_0^2 S_0^2}{2}$	$\frac{3a_4 C_0^2 T_0^2}{2}$
2p	$\frac{a_2 S_0^2}{2}$	$\frac{a_4 S_0^4}{2}$	$\frac{3a_4 S_0^2 C_0^2}{2}$	$\frac{3a_4 S_0^2 T_0^2}{2}$
2t	$\frac{a_2 T_0^2}{2}$	$\frac{a_4 T_0^4}{2}$	$\frac{3a_4 T_0^2 S_0^2}{2}$	$\frac{3a_4 T_0^2 C_0^2}{2}$
3r.	$\frac{a_3 C_0^3}{4}$			
3p	$\frac{a_3 S_0^3}{4}$			
3t	$\frac{a_3 T_0^3}{4}$			
4r.	$\frac{a_4 C_0^4}{8}$			
4p	$\frac{a_4 S_0^4}{8}$			
4t	$\frac{a_4 T_0^4}{8}$			

Case 4.1

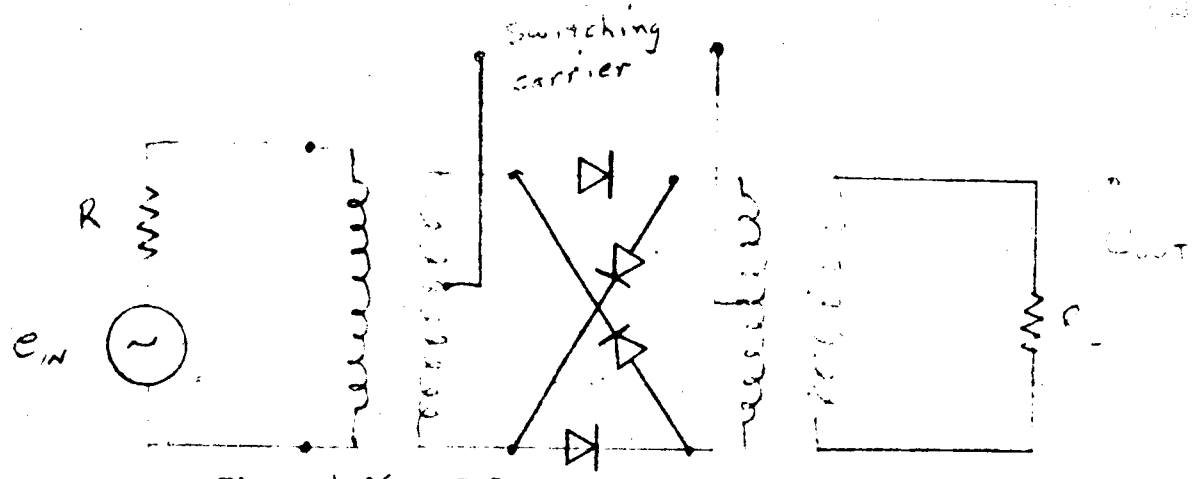

Figure 4.26. Balanced Mixer

The carrier is much larger than the input signal plus noise. The carrier sinusoid is converted to a square wave at the carrier frequency by the mixer diodes. The output spectrum is the input spectrum multiplied by the Fourier Series representation of the periodic carrier. It is useful to consider a modulation function, $\phi(t)$, which multiplies the input spectrum to yield the output. The modulation function is the reciprocal of the insertion loss of the modulator regarded as a time function since the loss varies as the instantaneous value of the carrier. Ideally, the modulation function is a symmetrical square wave which is represented by the Fourier Series

$$\frac{4\phi_m}{\pi} \sum_{n=1}^{\infty} \frac{\sin n\omega_c t}{n} \qquad (52)$$

where n is odd and ϕ m is the maximum height of $\phi(t)$ and w_c is the carrier frequency. The harmonic components of the series multiplied times the signal

spectrum yield the relative amplitudes of the modulated signal as nfc ± f where fc is the carrier frequency and f the signal frequency. Ideally the resulting spectrum is indicated in the simplified spectrum shown in figure 4.27.

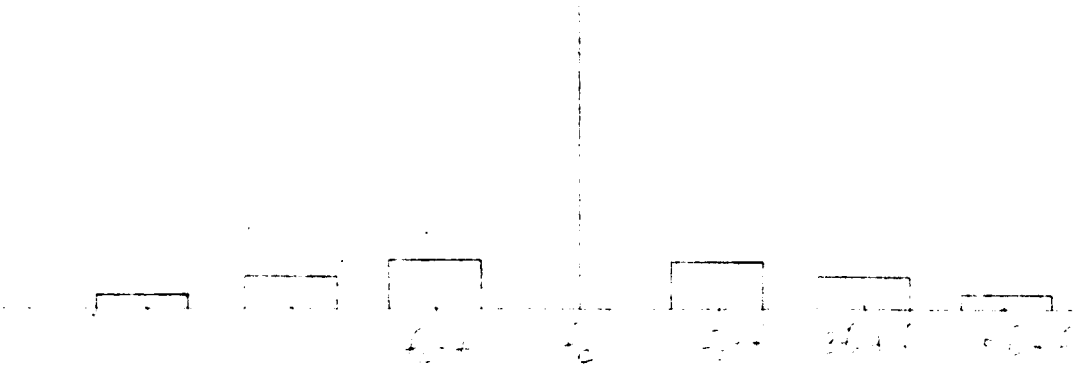

Figure 4.27. Translated Information Spectrum

The local oscillator and original input spectrum do not appear at the output. However, rejection of the local oscillator and signal spectrum is dependent on transformer balance and diode match. A practical limit of transformer balance is 40 DB (1%) as applied to the 60 mc circuitry of the input mixer. Diode balance has been improved with the introduction of the hot carrier diodes. However, a practical limit of narrow band carrier rejection by balance is approximately -30 DB. A practical limit on the broadband input signal spectrum rejection relative to the desired sideband output is approximately -20 DB. However, neither the carrier nor signal leak is particularly

objectionable as they fall outside the passband of the desired sideband. The products that combine and fall within the desired passband (as outlined in the power series case) are the components referenced in the specification. These components are a function of the signal drive level (as outlined in the case of the power series representation) and the mixer design. The Phase I limited experimental effort and past experience indicates that the spurious and feedthrough products within the information passband are limited to -50 DB with respect to the sideband of interest.

5.0 AGC Loop Design

The AGC specifications include the following: "The AGC loop gain shall be greater than 20 over its entire operating range such that the variation in the coherent receiver output, measured in the narrowband IF output shall not vary more than ± .3 DB for an input signal level variation of ± 6 DB about its design center". "The AGC loop filter shall be a passive single-pole RC low pass filter". "The AGC loop shall have four (4) standard loop noise bandwidths of .01, 0.1, 1.0 and 10 cps". The filter components shall be changeable and adhere to the component tolerances of par. 3.5.13.8C.

Initially the specified noise bandwidth and AGC loop gain is expressed as filter component values. A simplified AGC block diagram and derivation follow:

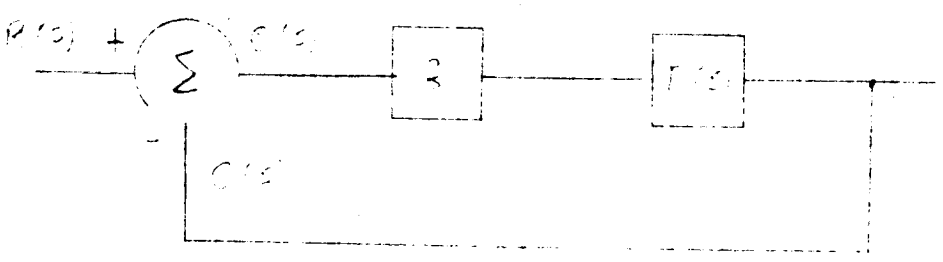

Figure 5.1 Simplified AGC Block Diagram

G is the dimensionless product of $K_D K_A G_1$ (K_D = Receiver IF Gain $\frac{db}{volt}$, K_A = coherent amplitude detector gain, $\frac{Volts}{db}$, G_1 = loop amplifier Gain, $\frac{Volts}{volt}$). A piecewise linear system is assumed.

$$F(s) = \frac{1}{\tau s + 1} \qquad \text{specified} \tag{53}$$

$$H_o(s) = GF(s) = \frac{G}{1 + \tau s} \tag{54}$$

$$H(s) = \frac{R(s)}{C(s)} = \frac{H_o(s)}{1 + H_o(s)} = \frac{G/1+\tau s}{1 + G/1+\tau s} \tag{55}$$

$$2B_L = \frac{1}{2\pi j} \int_{-j\infty}^{+j\infty} |H(s)|^2 \, ds \tag{56}$$

$$|H(s)|^2 = H(s)H(-s) = \frac{G^2}{(1+G)^2 - \tau^2 s^2} \tag{57}$$

$$I_n = \frac{1}{2\pi j} \int_{-j\infty}^{j\infty} \frac{g_n(s)}{h_n(s)\, h_n(-s)} \, ds \qquad \text{(from standard tables)} \tag{58}$$

$$= \frac{1}{2\pi} \int_{-j\infty}^{+j\infty} \frac{G^2}{[(1+G)+j\tau\omega][(1+G)-j\tau\omega]} d\omega$$

$$g_n(j\omega) = b_0(j\omega)^{2n-2} + b_1(j\omega)^{2n-4} + \cdots + b_n$$

$$h_n(j\omega) = a_0(j\omega)^n + a_1(j\omega)^{n-1} + \cdots + a_n \quad (61)$$

$$= (1+G) + \tau(j\omega) \quad (62)$$

$$\therefore \quad n = 1 \quad b_0 = G^2 \quad a_0 = \tau \quad a_1 = 1+G \quad (63)$$

$$b_1, b_2, \cdots b_n = a_2, a_3, \cdots a_n = 0$$

$$\therefore \quad 2B_L = \frac{b_0}{2a_0a_1} = \frac{G^2}{2\tau(1+G)} \quad (64)$$

$$\therefore \quad \tau = \frac{G}{2(2B_L)} \quad \text{for} \quad G >> 1 \quad (65)$$

5.1 Distribution of Loop Gain

The open loop gain G is specified as follows: "The narrowband IF output shall not vary more than ± 0.3DB as the input traverses ± 6DB change. Further the AGC loop gain shall be greater than 20 over its entire operating range". The Input Amplifier attenuation constant ($K_D \frac{db}{volt}$) and the coherent amplitude detector constant ($K_A \frac{volts}{DB}$) characteristics must be accurately known before an accurate design can be made. The following indicates the procedure with K_D and K_a assumed. K_D is assumed to be 12 DB/volt based upon the experimental performance of a single diode attenuator, interstage (one attenuator yielded 4DB/volt).

As indicated by line 6 column 18 of figure 2.3, the AGC amplifier noise input is -7.76 DBM when the carrier tracking loop is at threshold (S/N -28.4DB in predetection bandwidth). The AGC amplifier gain is 27.76DB; therefore, the quadrature phase detector noise power input is +20DBM and the signal power -8.24 DBM. Therefore, the AGC loop will regulate the quadrature phase detector signal input power at a nominal level of -8.24 DB. The estimated peak S curve of the quadrature phase detector at the -8.24DB

drive level is 250 mv. Further, $K_a \frac{\text{volts}}{DB}$ at the same drive level is estimated as .03 $\frac{\text{volts}}{DB}$. If the total dynamic range of the diode attenuator control voltage extends from -2 to -7 volts to produce minimum to maximum attenuation, the AGC loop DC amplifier gain is tentatively established as outlined in the following table.

1.	Range of Input Signal Level (DBM)	-54 to -84
2.	Output Variation over Input Signal Level Range (DBM) (0.3DB regulation for 6DB change of input)	-8.24 to -9.74
3.	AGC Quadrature S curve (v peak)	-0.250 to -0.205
4.	AGC Voltage Range Receiver Control Voltage	-7 to -2

Table. 5.1 AGC System Dynamic Voltage Ranges

The required loop amplifier gain (G_1) is simply line 4 divided by line 3 or 110. The numerical loop gain (for the previously mentioned assumptions) becomes

$$G = K_A \frac{\text{volts}}{\text{db}} \cdot K_D \frac{\text{db}}{\text{volts}} \cdot G_1 \frac{\text{volts}}{\text{volts}}$$

$$= 10 \frac{\text{db}}{\text{volt}} \cdot 0.22 \frac{\text{volts}}{\text{db}} \cdot 1.0$$

$$G = 2.2$$

The loop filter time constants are listed in table [redacted]. The AGC loop is non-linear and the loop gain of 40 is maximum. The loop gain is a function of the signal strength (the loop gain is zero when the received signal power is zero). The gain controlled amplifier attenuation constant K_D is the principal non-linear element in the loop. The specification states that the minimum loop gain must be at least 20 at minimum signal strength. Therefore, the allowed variation of K_D from maximum to minimum signal strength is two. If this variation cannot be maintained, the loop gain at maximum signal strength must exceed 40 such that the minimum loop gain is 20. The quadrature phase detector scale factor, K_a, is also non-linear. However, if the loop

$$\omega_1 = \frac{1}{\tau} = \quad = (2\pi B_L)$$
$$G$$

$$K_P = \lim_{S \to \infty} K_0 \left(\quad + \quad G\right.$$

$2B_L$ (cps)	G (sec^{-1})	K_P	ω_1 (rps)	τ (sec)
0.01	40	40	5×10^{-4}	2000
0.1	40	[illegible]	5×10^{-3}	200
1.0	[illegible]	[illegible]	5×10^{-2}	20
[illegible]	[illegible]	[illegible]	5×10^{-1}	[illegible]

TABLE 5.2 AGC LOOP FILTER PARAMETERS

gain regulates the signal level variation at the quadrature phase detector within approximately 3DB, K_a is assumed linear.

This simplification is similar to the APC loop assumption that the phase detector constant is linear if the phase error is regulated within $\pm$ 30 degrees.

The quadrature phase detector scale factor K_a was assumed to be .03 $\frac{\text{volt}}{\text{DB}}$. Figure 5.2 is a repetition of the demodulation channel phase detector transfer of peak to peak beat frequency output as a function of signal drive level. The noise power input is +20DBM at AGC loop threshold. The equivalent peak beat note (which corresponds to the DC output when the VCO is in lock) is approximately 6.25 volts. The signal power is -28.4DB with respect to the noise power; therefore, the quadrature phase detector DC output is -28.4DB with respect to 6 volts or 242 mv. A one DB change from 242 mv is 28.2 mv (K_a was assumed to be 30 $\frac{\text{mv}}{\text{volt}}$).

5.2 AGC Loop Mechanization

The AGC loop components have been discussed previously in the report except the Input amplifier which is described in section 6.0.

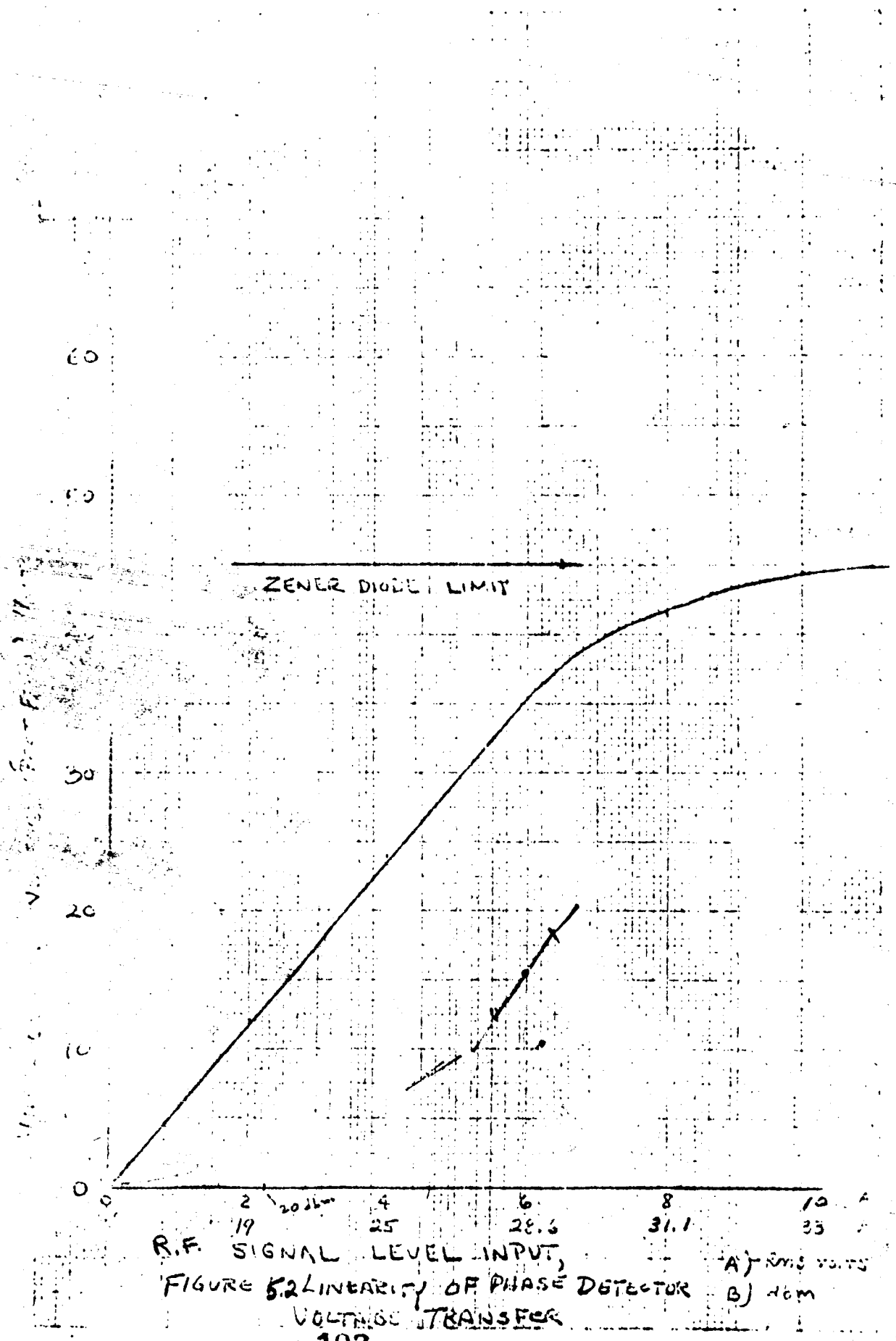

FIGURE 5.2 LINEARITY OF PHASE DETECTOR VOLTAGE TRANSFER

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5.3 AGC Loop Filter Components

As shown in table 5.2 the AGC loop filter time constants range from 2 sec. to 2000 sec. The simple low pass filter arrangement shown in figure 5.3 is one solution. The specification states that a passive filter must be implemented. Unfortunately, a passive filter is subject to loading; therefore, an operational amplifier connected as a follower maintains a high load impedance for the loop filter. If an active filter is acceptable, the loop amplifier and filter can be combined, eliminating one operational amplifier and the filter loading.

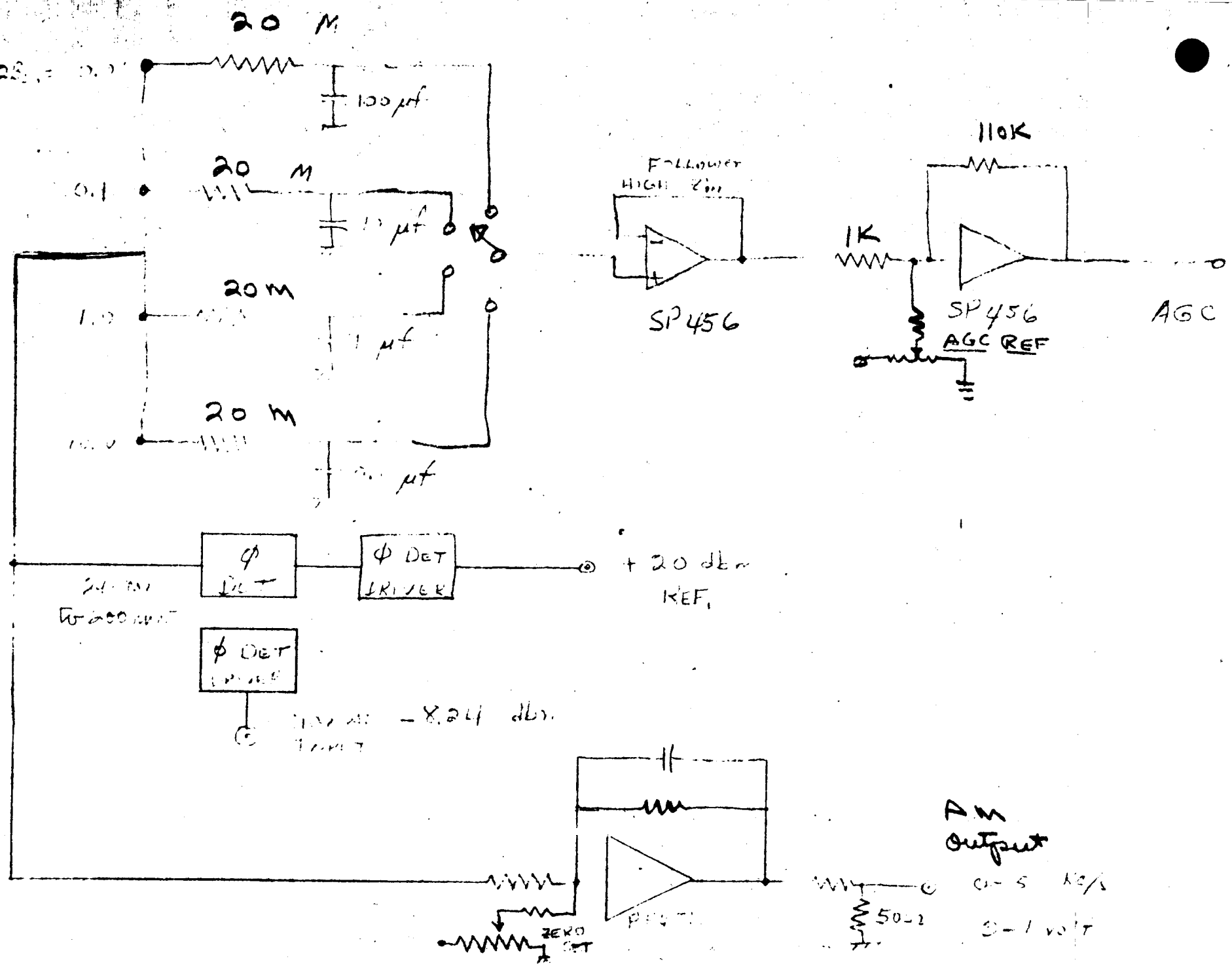

Fig. 3.3 AGC Networks

6.0 Input Amplifier

The principal Input amplifier Specs include the following:

1. Center Frequency	50MC
2. 3DB Bandwidth	10MC
3. Response	+ 0.25DB within 2MC of 50MC
4. Phase Linearity	Compatible with Fidelity Spec.
5. AGC Response	Compatible with S/N Dynamic Range

The PM receiver level diagram outlined in Figure 2.3 lists the Input amplifier characteristics. The required gain is 30DB, AGC range 30DB, 3DB bandwidth 10MC and linear power capability 0DBM. The Input Amplifier shall consist of four cascaded Feedback pairs. The principal parameters of this unit include the following:

1. 3DB Bandwidth	1KC - 80MC
2. Noise Figure	9DB(Max Gain)
3. Power Gain	10 to 25DB depending on Feedback connection

4. Gain Stability — 1DB oven temperature -55°C to +100°C

5. Linear Small Signal Power Capability -10DBM

The frequency response of the Input Amplifier will be established by a passive input filter. The filter shall meet the ± 0.25DB requirement over the band 48 to 52MC with a minimum 3DB bandwidth of 10MC. However, aside from these specified requirements the filter will have a linear phase characteristic.

The AGC range will be achieved by Feedback pair interstage diode attenuators. The design goal overall gain of the unit including the insertion loss of the interstage attenuators at AGC threshold is 30 DB. Figure 6.1 indicates a simplified diagram of this system. The attenuators yield up to 10 DB attenuation for the range of applied AGC voltage -1 to -4.5 volts.

This system minimizes the usual problems of maintaining bandpass and phase characteristics over the AGC range.

6.1 Noise Figure Considerations

The Input Amplifier, interstage diode attenuator system associated gains

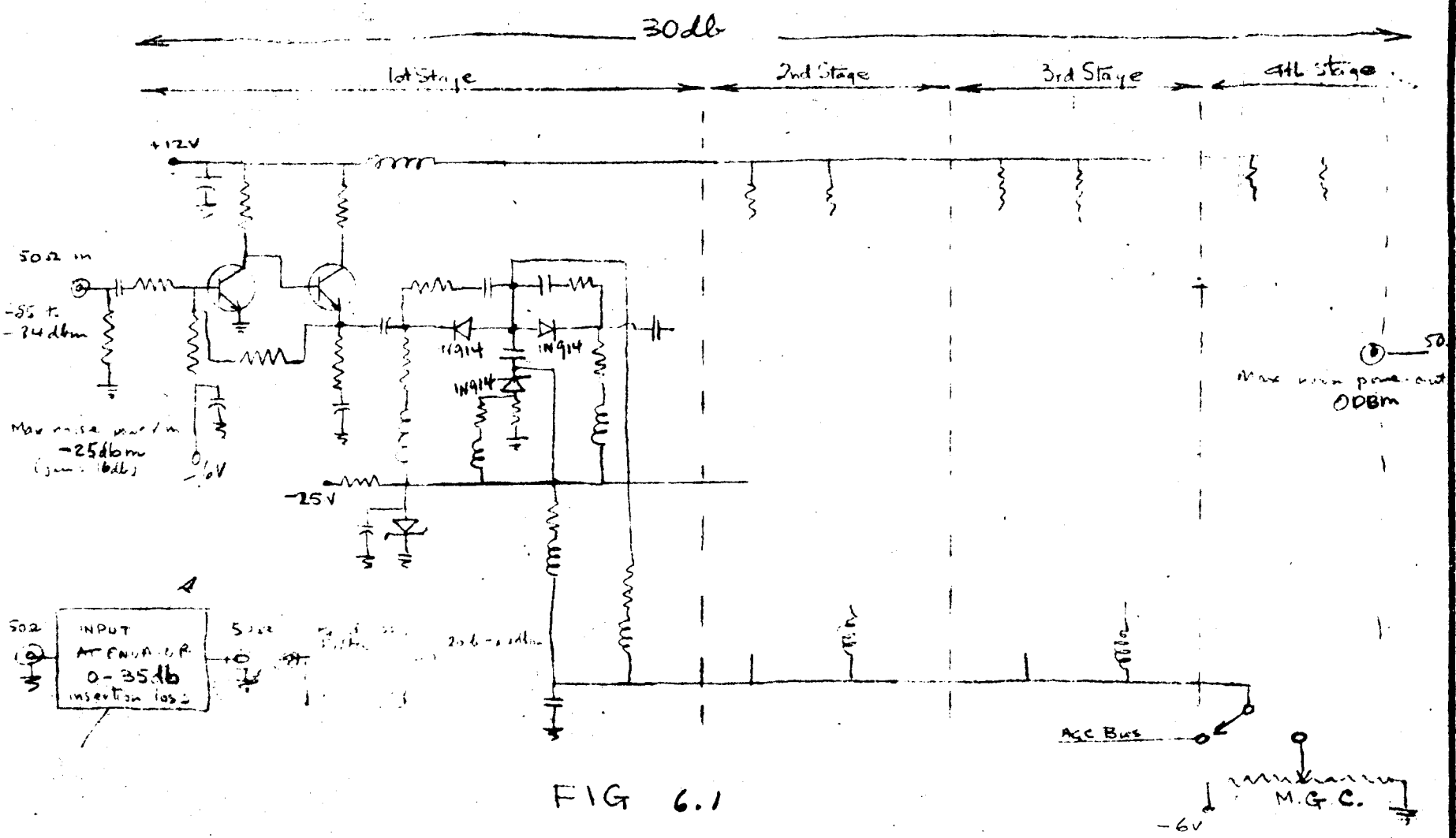
30db
1st Stage
2nd Stage
3rd Stage
4th Stage
+12V
50Ω in
-55 to -24dbm
Max noise power in -25dbm
(gain = 6db)
0 to -6V
IN914
IN914
IN914
-25V
50Ω
Max noise power out 0DBm
50Ω
INPUT ATTENUATOR 0-35db insertion loss
AGC Bus
M.G.C.
-6V

FIG 6.1

and losses is shown in Figure 6.2.

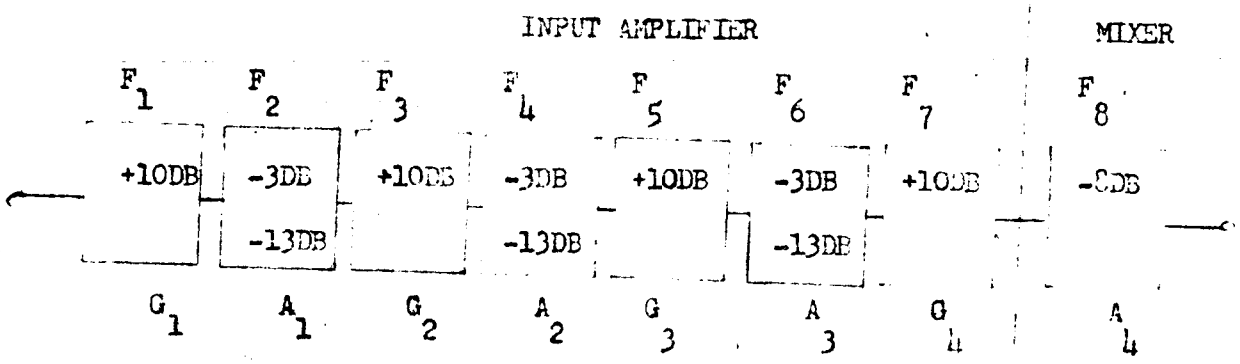

Figure 6.2. Input Amplifier and Mixer Noise Figure Characteristics

The forward gain of the four cascaded feedback pairs is +40DB. The minimum insertion loss of the three diode attenuators is -9DB and the maximum insertion loss -39DB. The mixer noise figure and conversion efficiency is assumed to be 15DB and -8DB respectively.

The overall noise figure at maximum gain is as outlined by the equation below.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 A_1} + \frac{F_4 - 1}{G_1 A_1 G_2} + \frac{F_5 - 1}{G_1 A_1 G_2 A_2} + \frac{F_6 - 1}{G_1 A_1 G_2 A_2 G_3} + \frac{F_7 - 1}{G_1 A_1 G_2 A_2 G_3 A_3} + \frac{F_8 - 1}{G_1 A_1 G_2 A_2 G_3 A_3 G_4}$$

The Feedback Pair noise figure is 8DB. The diode attenuator noise figure is assumed as 8DB. The mixer noise figure is assumed as 15DB.

F_1 through F_7 = 6.3

F_8 = 31.7

G_1 through G_4 = 10.0

A_1 through A_3 = 0.5

A_4 = 0.11

The maximum gain noise figure is 9DB. At minimum gain, the following changes are apparent.

F_1 through F_7 = 6.3

F_8 = 31.7

G_1 through G_4 = 10

A_1 through A_3 = 0.05

A_4 = 0.11

The minimum gain noise figure is approximately 20DB.

Measurements taken on a similiar system indicated a 10DB noise figure at maximum gain and 24DB at minimum gain.

The noise power in (KTB) in 1 cps bandwidth is-174DBM. The receiver noise figure degrades this by 2NDB (at minimum gain) to-150DBM. However, the minimum power from the S/N Summer in 1 cps bandwidth is -124.75DBM. Therefore, the receiver noise power is -25.24DB with respect to minimum Summer noise.

7.0 Wideband Demodulation Channel

The block diagram and associated signal and noise power levels of the demodulation channel are shown in figure 2.4. The Demodulation Channel signal and noise power levels were discussed in section 2.4.

7.1 Demodulation Channel Input Filter

As specified "The wideband IF amplifier shall have a minimum 3DB bandwidth of 6 mc and shall be flat to within $\pm$ 0.5 db within $\pm$ 1.5 mc of the center frequencies. Its phase response shall be symmetric within $\pm$ 5^{o} over the 6 mc passband and sufficiently linear to meet the fidelity requirements of par. 3.5.1.1.3.

The demodulation channel bandwidth and phase response will be determined primarily by the input filter. The succeeding amplifiers will be broad band feedback pairs. The filter design will adhere to the specified amplitude response ($\pm$ 0.5 DB within $\pm$ 1.5 mc of center frequency), and specified phase symmetry. Because of the large percentage bandwidth (60%), ordinary low pass to bandpass transformation cannot be used. Such a design will yield geometric not arithmetic symmetry. However, Westinghouse has a design procedure whereby correction terms are added to the characteristic

function and arithmetic symmetry obtained for all frequencies within and somewhat beyond the passband. However, in our opinion the filter should have a linear phase response (Bessel). The resulting 3DB bandwidth will extend beyond 6 mc. The amplitude response and group delay of a 4 pole Bessel filter designed with 0.2 DB amplitude droop 1.5 mc from center frequency is indicated in figures 7.1 and 7.2.

7.2 Wideband Demodulation Channel Distribution Amplifier, Limiter and Phase Detector Driver

The distribution amplifier provides a 3 DB power split between the predetection record and the demodulation channel with an overall gain of 4DB. Two feedback pairs with an input resistive power divider will constitute the distribution amplifier.

The demodulation channel limiter will be essentially the same as the tracking loop limiter described in section 4.9 except that the nine limiter stages will be used instead of seven.

7.3 Demodulation Channel Phase Detector

The high power phase detector developed in Phase I (described in par. 4.2) will constitute the demodulation channel phase detector. A repetition of the phase detector video output vs signal drive characteristic

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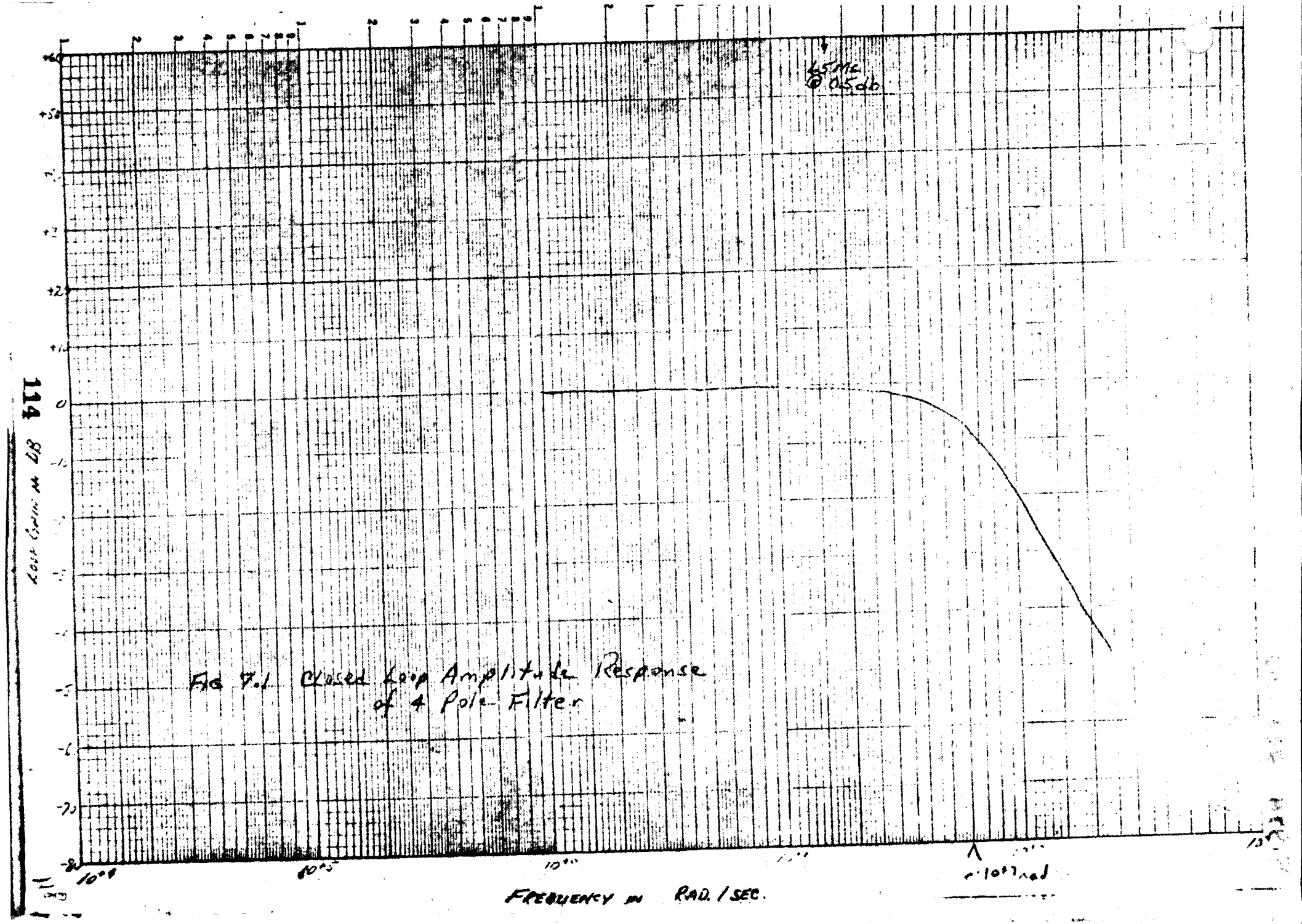

Fig 7.1 Closed Loop Amplitude Response of 4 Pole Filter

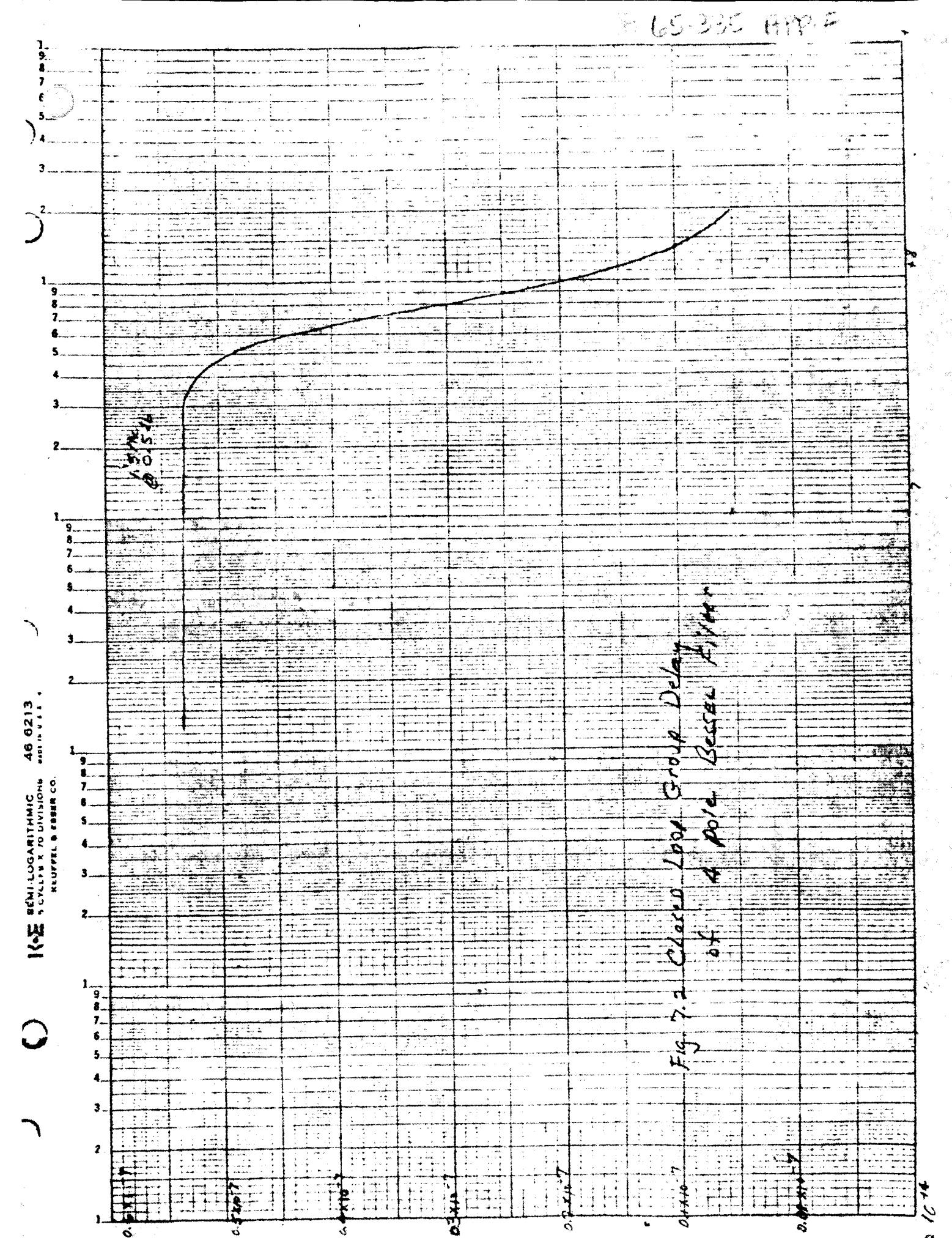

Fig. 7.2 Closed Loop Group Delay of a Pole Bessel Filter

is shown in figure 7.3. As shown in column 21 of figure 2.4 (Demodulation Channel Level Diagram) the phase detector signal drive level is 20DBM.

As shown by figure 7.3, 20 DBM signal drive corresponds to 12.5 volts peak to peak video. (The unit is linear to 28.6 DBM drive). However, the unit is required to operate with a S/N of -40DB in the predetection bandwidth. Therefore, the Phase Detector video output will be 40 DB down from 12.5 or 125 mv peak to peak.

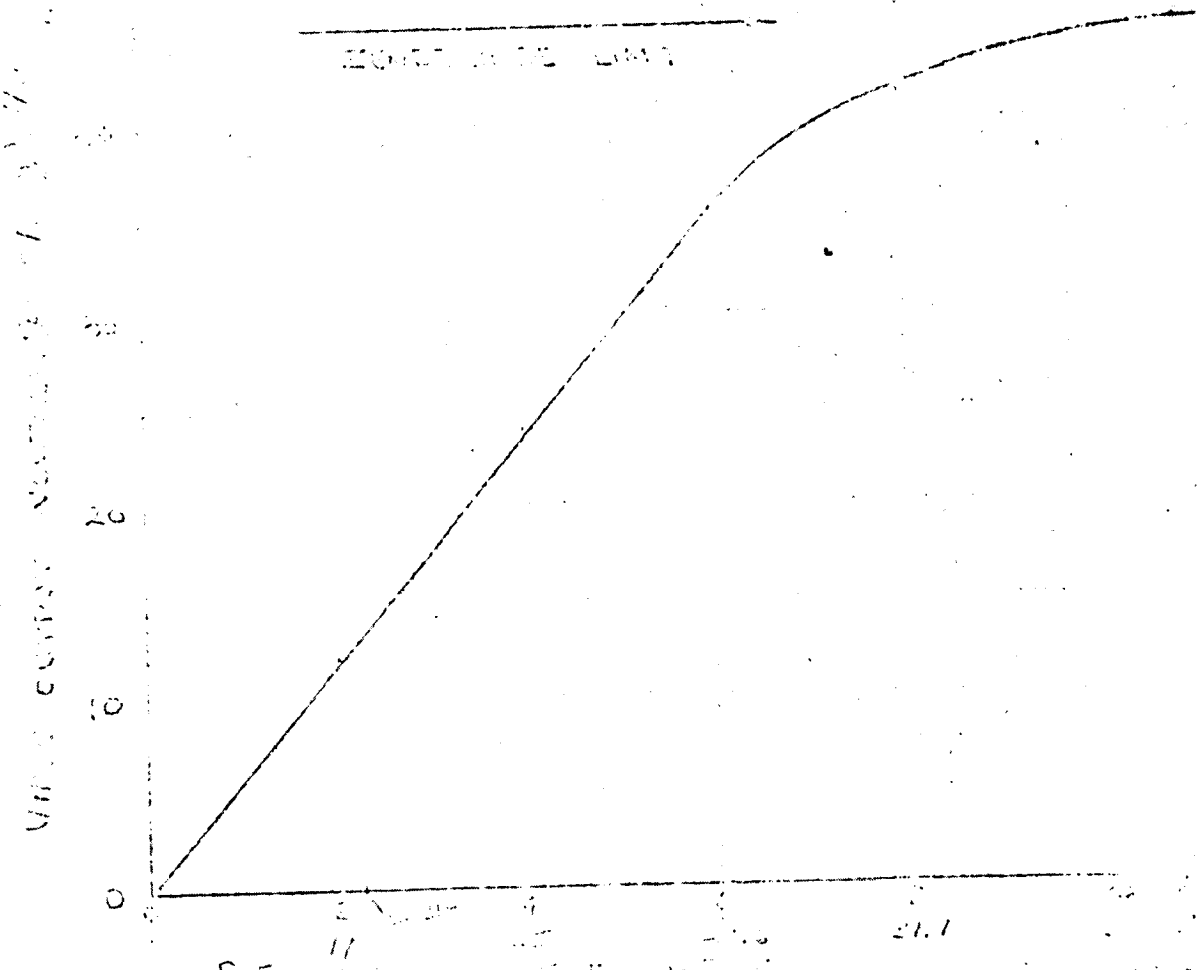

FIGURE 7.3

8.0 Predetection Record

The predetection record system is outlined in Figure 2.1. This system deviates from the specified block diagram of figure 3 JPL Spec. GPC 15062-DSN for the following reasons. Figure 8.1 indicates the wideband demodulation channel spectrum if the full 6 mc channel bandwidth is used. Further, the same figure indicates the modulator output as the wideband channel is down converted by the 15 mc local oscillator.

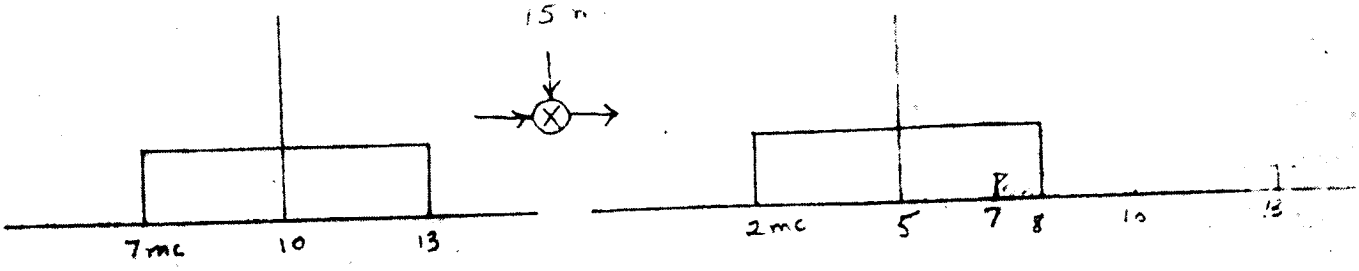

Figure 8.1 Predetection Record Spectrums

Note that the modulation mixer feedthrough overlaps the record spectrum centered on 5 mc. The balanced mixer rejection of the original modulation centered on 10 mc is typically 20DB. The recorded spectrum will include an overlapping region. If the wideband demodulation spectrum does not extend from 7 to 13 mc but rather 8.5 to 11.5 mc as the PM Transmitter Specs indicate, then the

above assumption is erroneous.

If the full 6 mc capability of the wideband channel is used and overlap must be avoided an additional stage of up conversion and down conversion is recommended. The spectral distribution of this system is shown in figure 8.2.

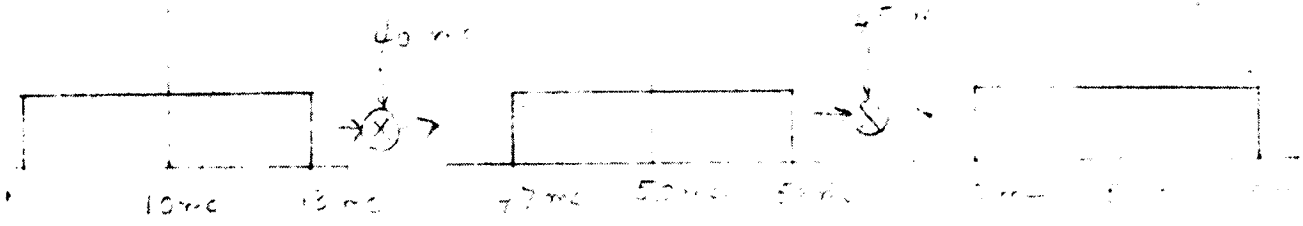

Figure 8.2. Predetection Record Spectrum with an Additional Stage of up Conversion and Down Conversion.

The Predetection Recorded spectrum is taken from the wideband channel prior to the limiter. Therefore, the recorded data is not subjected to limiter suppression.

A simplified diagram of this system is shown in figure 8.3.

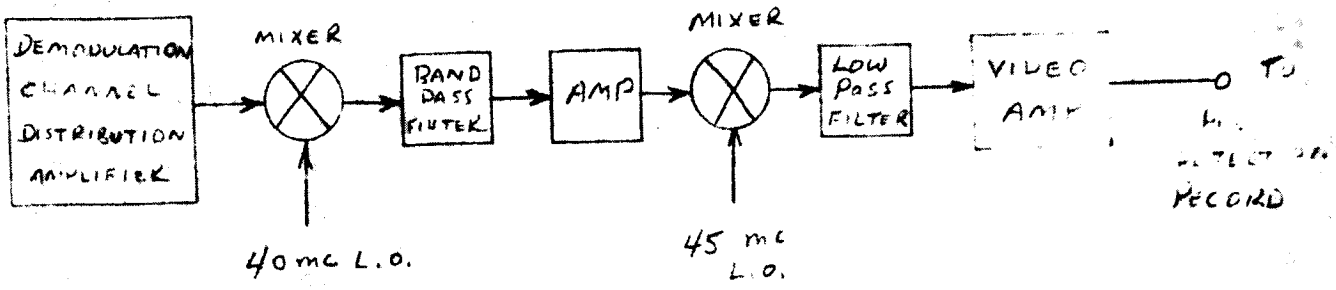

Figure 8.3.

The Predetection Record system implemented will be determined by the cognizant engineer's decision on the maximum required demodulation channel spectrum bandwidth.

9.0 Predetection Playback

The predetection playback system outlined in par. 3.5.1h and figure 5 of JPL Spec GPG-15062 is summarized briefly as follows: The tracking loop VCO is switched from 60 mc to 15 mc and the predetection record spectrum centered on 5 mc is multiplied by 15 mc for processing in the 10 mc tracking and demodulation channels. In our opinion, this system has two faults. 1) The signal spectrum and the up converted spectrum are shown in figure 9.1.

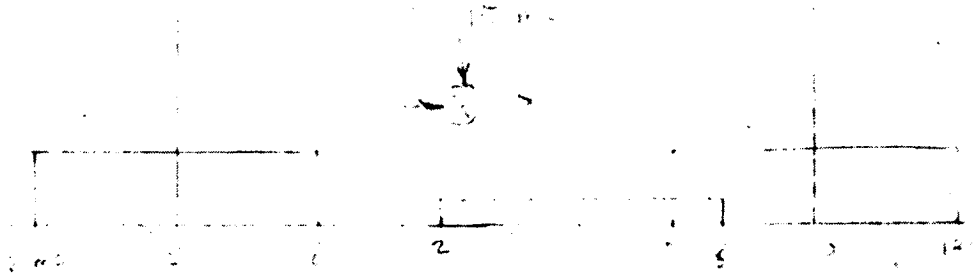

Figure 9.1. Predetection Playback Spectrums

As shown any signal spectrum that leaks thru the mixer overlaps the up converted spectrum center on 10 mc. Further, any second order component of the playback (attributed to distortion in the tape recorder) that leaks through the mixer will fall within the 10 mc passband of the tracking loop and wideband 10 mc IF amplifiers. The obvious solution is to simply build the balanced

mixer for 60 DB rejection of all signal components and 60 DB rejection of the local oscillator. Local oscillator (single frequency) rejection of -40 DB is considered practical and possibly -50 DB with hot carrier diodes; however, to achieve and maintain this order of balance over the 6 mc signal bandwidth is beyond the state of the art. The typical broadband signal rejection attributed to balance is about 20 DB. A system that avoids the mixer balance problem is outlined in figure 2.1, the PII Receiver Block Diagram, and repeated in figure 9.2.

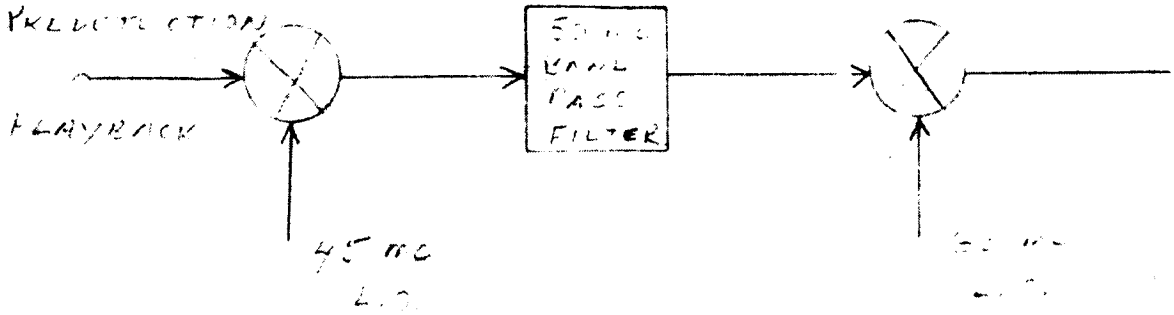

Figure 9.2. Block Diagram Modified Predetection Playback System

The signal spectrums associated with this diagram are shown in figure 9.3.

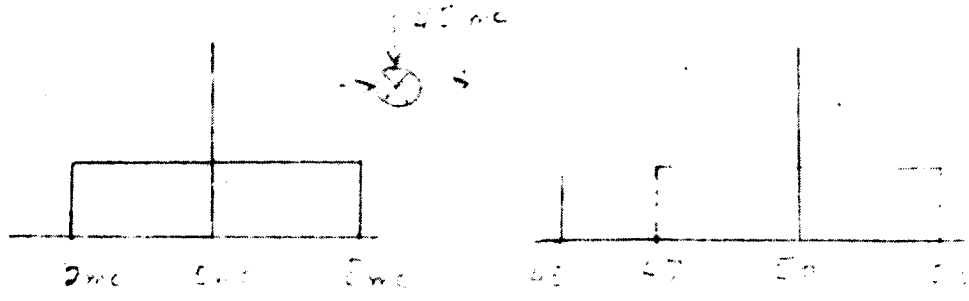

Figure 9.3. Predetection Playback Spectrums with an Additional Stage of Up Conversion.

This system does not solve the limitations of mixer balance but rather spreads the spectrum such that the mixer feedthrough is rejected by the intermediate bandpass filter. However, in all fairness this system has the disadvantage of rejecting the 45 mc LO (which is only 2 mc removed from the up converted signal spectrum). However, as outlined earlier single frequency rejection or balance is easier to maintain that broadband balance.

10. Frequency Synthesizer

The Frequency Synthesizer block diagram is shown as a portion of figure 2.1, the P.M. Receiver Block Diagram. As outlined earlier, the Reference Oscillator is mechanized as a 1mc oscillator X5, X2 frequency multipliers. The resulting 10 mc is distributed as the reference to the tracking loop phase detector, the demodulation channel Phase Detector and the AGC quadrature phase detector. Further, the 40 and 45 mc Predetection Record and Predetection Playback mixer references are derived from the 10 mc reference source.

The 1 mc oscillator and frequency multiplier designs have been described in earlier sections. The contemplated 10 mc distribution amplifier is outlined in figure 10.1. The 10 mc distribution amplifiers provide unity power gain and drive three 360 degree phase shifters (Varigon Series V54). The phase shifter insertion loss is 30 DB. The phase shifters are buffered from the various phase detectors by power amplifiers with 37 DB gain delivering +20 DBM. The power amplifiers will be phase and gain stable units similar to the tracking 1 op second IF stages. The frequency synthesizer power and impedance levels are shown in figure 2.1.

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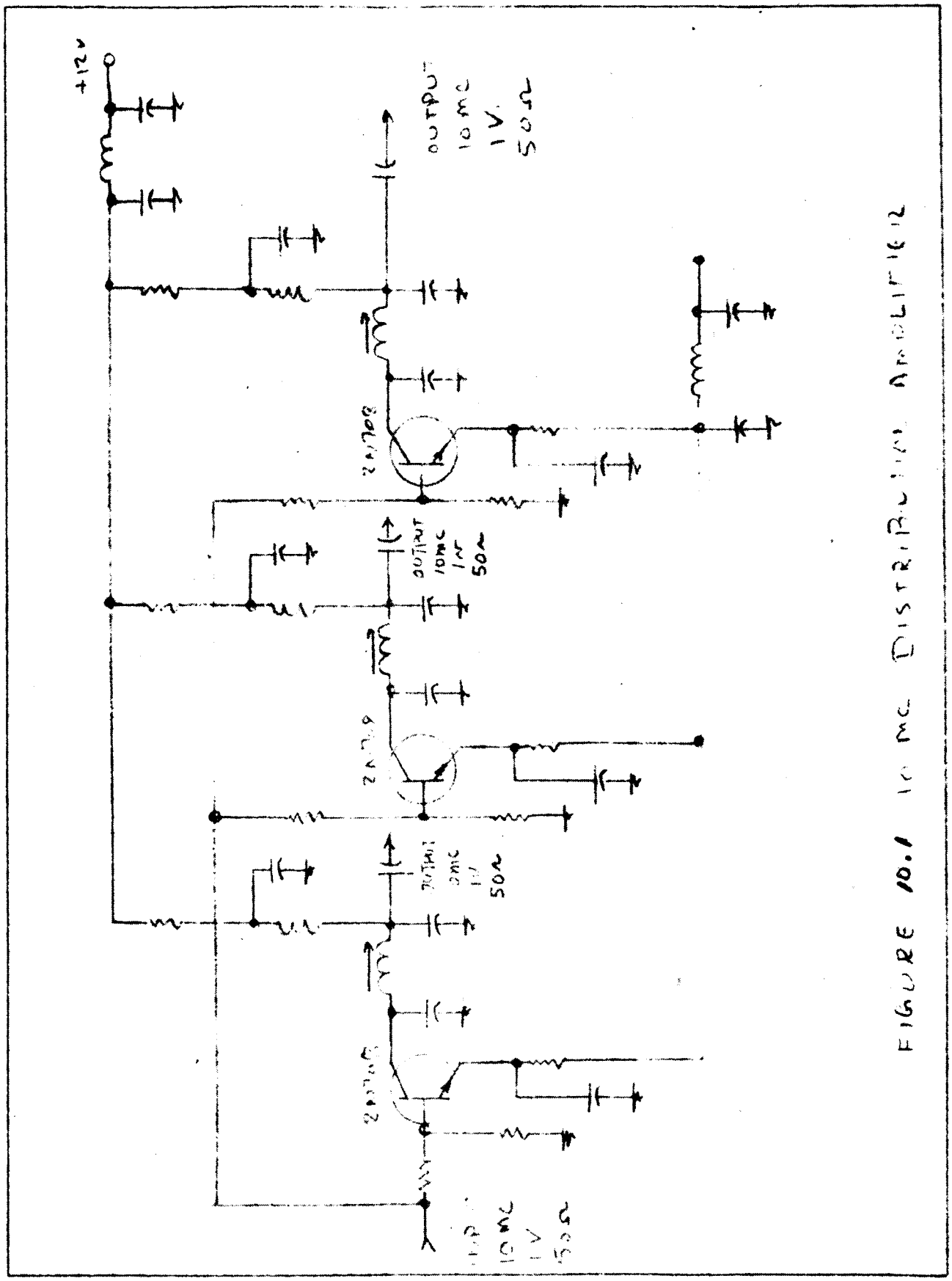

FIGURE 10.1 10 MC DISTRIBUTION AMPLIFIER

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11.0 Output Amplifiers

The output amplifiers as shown in figure 2.1, the FM Receiver Block Diagram, are listed as follows:

1. Narrow Band Modulation output amp.
2. Wideband Modulation output amp.
3. AM Modulation output amp.
4. Predetection Record output amp.

The units 1 thru 3 will be Philbrick SP 456 stabilized operational amplifiers. The predetection record amplifier will be a medium power feedback pair discussed earlier in this report.

receiver tracking loop gain.

3.5.1.3.3 Balanced Modulators

The PM receiver shall contain two (2) balanced modulators, as shown in figure 2.1. They shall be functionally equivalent to ideal voltage multipliers in the time domain, or translators in the frequency domain, such that all spurious and feedthrough products are 50DB below the desired output. The referenced spurious and feedthrough products are referenced to the output of the tracking loop 2KC filter and the demodulation channel 6MC filter and are referenced to the 2KC and 6MC bandwidths respectively.

3.5.1.3.4 IF Amplifiers

a. Narrowband IF

The wideband and narrowband IF amplifiers will track in phase within $\pm 5^{\circ}$ over $\pm$ 33 cps. about the center frequency. At center frequency, the tracking will be within 20 degrees as determined by the limiter and AGC phase shift over the dynamic range of the system, but it will be possible to manually adjust out this phase error with the reference phase shifter.

3.5.1.3.2 Voltage-Controlled Oscillator

a. Frequency

The center frequency of VCO No. 1 shall be exactly 60MC. The VCO center frequency shall be 1MC. The final 60MC frequency shall be derived by X60 frequency multiplication of the VCO frequency.

b. Stability

The frequency and phase stability of the VCO, Reference Oscillator and Transmitter Standard shall be such as to cause no more than a one (1) degree RMS phase error in a noise-free phase coherent receiver with 2BL of 3.0 cps when the three oscillators are at center frequency.

c. Manual Tuning

It shall be possible to manually tune the VCO for the purpose of initially acquiring the transmitter frequency and for subsequently creating controlled loop static phase errors as large as $\pm$ 30° during system testing. The afore referenced static phase error shall be achieved by $\pm$ 500 cps detuning of either the transmitter standard or receiver VCO and reduced

12.0 Specification Exceptions

The Phase I PM Receiver Study indicates that the following specification deviations and additions are appropriate.

3.5.1.3.1 Input Amplifier

a. Bandwidth

The passband of the 50MC Input Amplifier shall be flat to within ± 0.25DB within ± 2MC of the center frequency at mid range gain of the Input Amplifier. The passband shall not vary more than 1DB (over the ± 2MC passband) as the Input Amplifier traverses its full range of gain control.

b. Phase Linearity

The Input Amplifier shall have a Bessel Phase Response and amplitude response as described in 3.5.1.3.1a. The 3DB bandwidth is determinated by the specified amplitude response ± 2MC from center frequency and the phase response.

c. AGC Response

The gain of the Input Amplifier shall be AGC controlled over a range of 30DB. Manual gain control (independent of the Input Amplifier) shall extend the total PM Receiver gain control (AGC and Manual) to 65DB.

3.5.1.3.5 The PM receiver reference oscillator shall have a fixed-frequency output of exactly 10MC. The reference oscillator center frequency shall be 1MC. The final 10MC frequency shall be derived by X10 frequency multiplication of the reference oscillator frequency.

3.5.1.3.6 Phase Detectors

The PM receiver shall have two (2) phase detectors with the following characteristics.

a. Bandwidth

The tracking loop phase detector bandwidth shall be such that the one sided output passband is determined only by the 2KC IF passband. The demodulation channel phase detector 3DB bandwidth shall be a minimum of 5MC. The amplitude response at 1.5MC shall be within 0.5DB of the response at DC.

b. Fidelity

The phase detectors shall be functionally equivalent to ideal voltage multipliers in the time domain consistent with the transmitter-receiver fidelity specification of 3.5.1.1.3.

3.5.1.3.8 Loop Filter

The phase-lock PM receiver shall have the following loop characteristics:

a. The receiver shall have four standard loop noise bandwidths of 3, 12, 20 and 45 cps in the passive configuration defined at the receiver absolute threshold SNR operating point (ODF SNR in tracking loop noise bandwidth). It shall be possible to simply and reliably change the loop filter components in order to operate with either the same bandwidths at different defined threshold points or with any other loop noise bandwidths from 1 to 1000 cps. The lowest operational noise bandwidth at threshold, defined as ODF SNR in the noise bandwidth, shall be 3.0 cps. Further, at noise bandwidths greater than 100 cps the 2KC tracking loop, IF crystal filter must be changed or the resulting degradation of loop stability accepted.

3.5.1.3.9 Amplitude Detector

a. Linearity

the fidelity specification is referenced to distortion above and beyond the inherent distortion of a sinusoidal phase detector to an input signal with a modulation index of ± 4.

c. Gain Constant

Each phase detector shall contain a hard limiter such that its gain, measured in volts/radian, shall not vary more than $\pm \frac{1}{2}$ percent over 36DB of limiting in the tracking loop and 40DB of limiting in the demodulation channel. Further, the relative phase shift between the tracking loop and demodulation channel attributed to changes of limiting dynamic range shall not exceed 20 degrees and will be possible to null it out manually.

3.5.1.3.7 Phase Loop Gain

The PM receiver loop gain shall be sufficiently large such that the residual phase error shall be no greater than 1 degree over the normal receiver operating frequency range as determined by the transmitter tuning range and the frequency instabilities, when the VCO is tuned to its zero-voltage quiescent frequency.

The relationship between carrier input voltage amplitude and detector output voltage shall be linear to with ± 2.5% under both static and dynamic conditions.